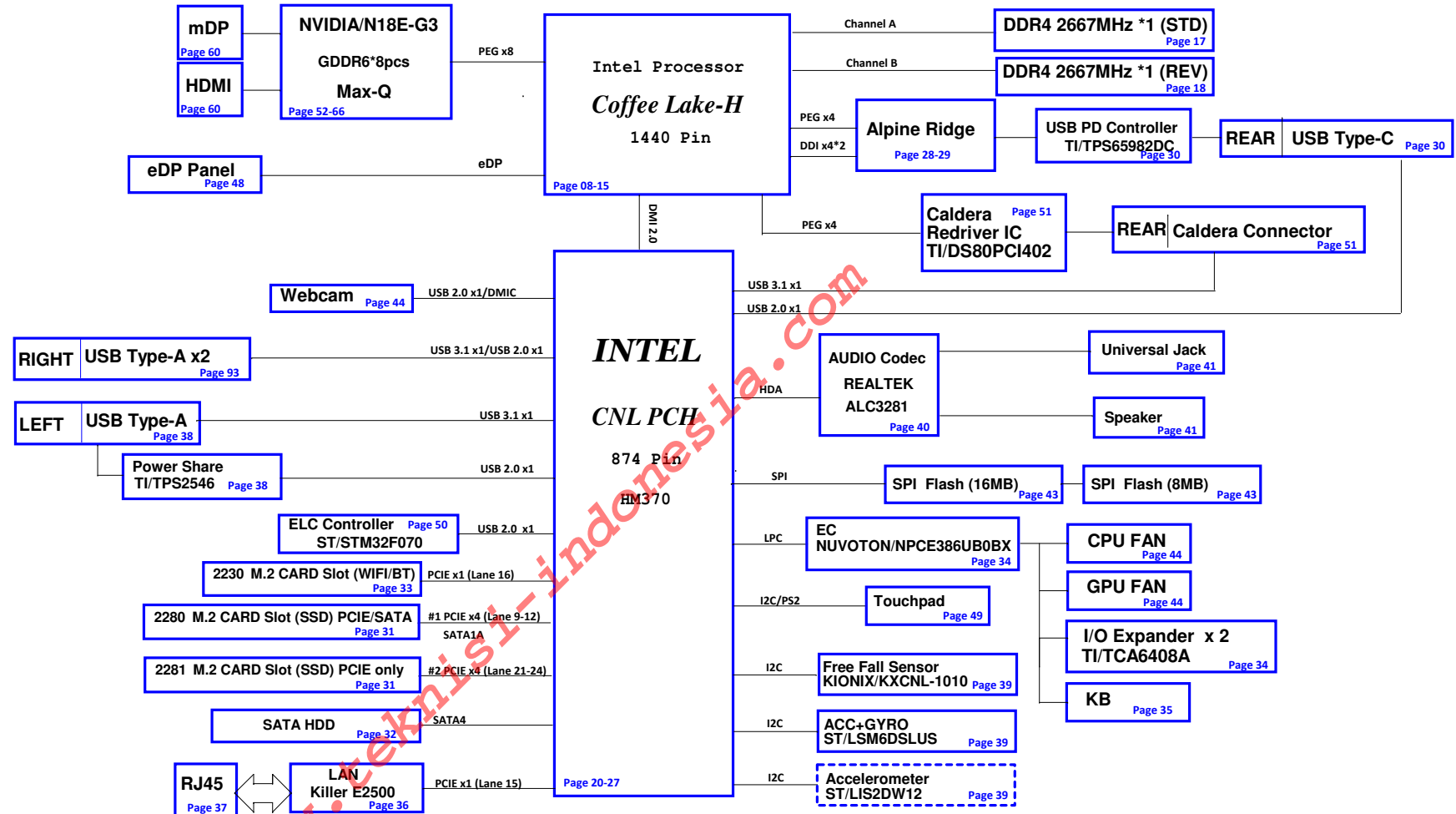


Orion N18E G2/G3-MaxQ (Coffee Lake-H)

Revision_X00

SO-DIMM (support max memory up to 32GB)

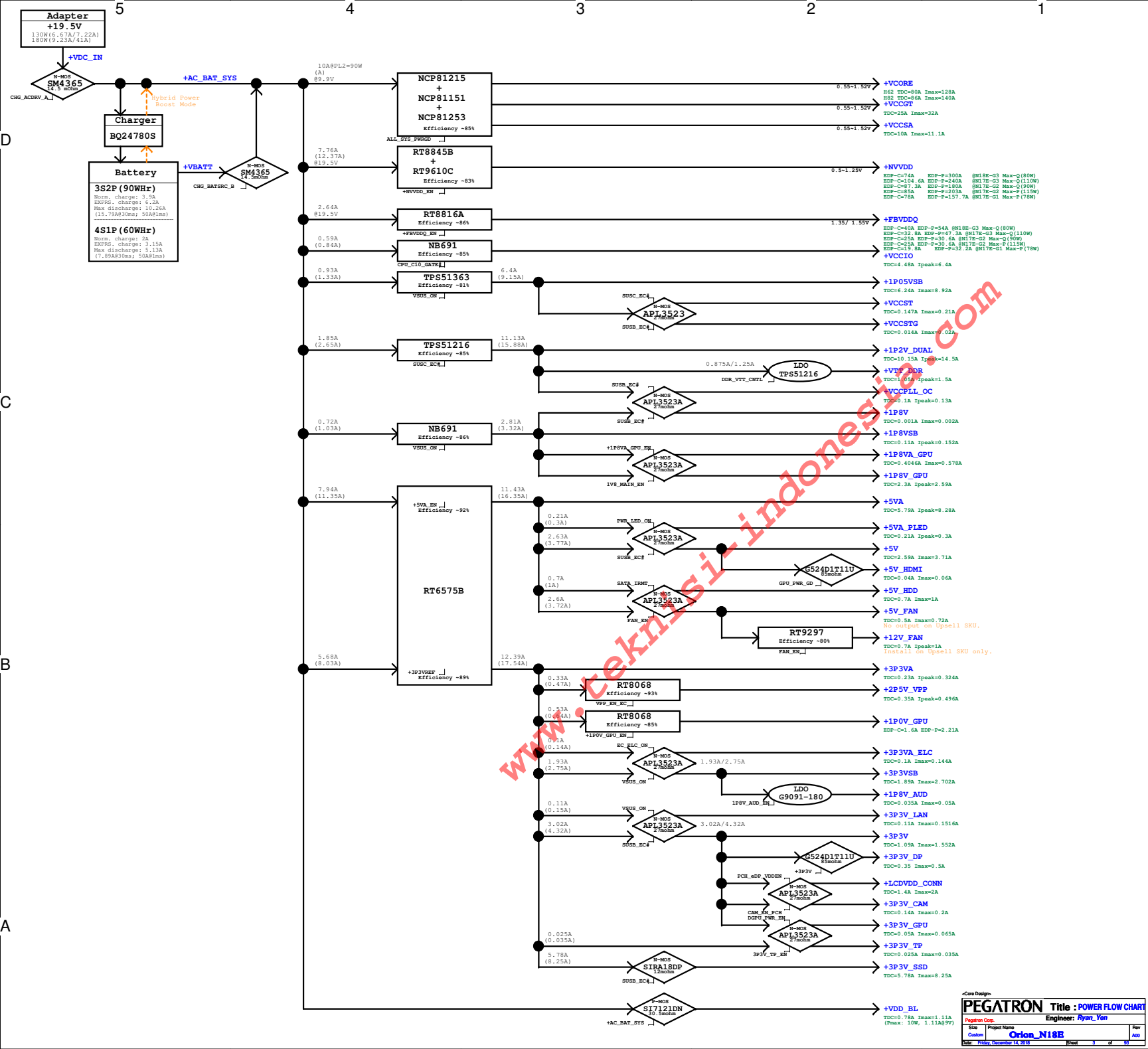


PAGE	TITLE
01	BLOCK DIAGRAM
02	SIGNAL & RESET MAP
03	POWER FLOW CHART
04	CHANGE HISTORY
05	SMBus & I2C Flow
06	GPU Power flow & sequence
07	POWER SEQUENCE
08	CPU DDI/EDP
09	CPU DDR4 CHA
10	CPU DDR4 CHB
11	CPU PCIE/DMI
12	CPU other
13	CPU VSS
14	CPU VCC
15	CPU DECOUPLING
16	ME DISABLE
17	DDR4_SO-DIMM0
18	DDR4_SO-DIMM1
19	DDR4 DECOUPLING
20	PCH DMI PCIE_USB_SATA
21	PCH SATA/PCIE
22	PCH ESPI/SPI/FAN/HOST
23	PCH AUDIO/CL/I2C/UART
24	PCH SML/I2C/MISC
25	PCH CLOCK
26	PCH VCC/PLL
27	PCH VSS
28	Alpine-Ridge - Controller
29	Alpine-Ridge - Power
30	Alpine-Ridge - PD
31	M.2 2280 SSD #1 & #2
32	SATA HDD
33	M.2 KEY-A 2230 WLAN
34-35	EC_NUVOTON_NPCE386UB0BX
36-37	LAN NIC KILLER & LAN JACK
38	USB CONN and power
39	SENSOR
40	AUDIO CODEC ALC3281
41	AUDIO JACK
42	USB Redriver
43	SM BUS & SPI ROM
44	Other Conn
45-46	PCH/CPU DEBUG TESTPOINT
47	PCB & Label & Screw
48	eDP Conn
49	Touch & Keyboard BL
50	ELC MCU
51	Caldera Redriver & CONN
52	GPU PCIE
53	GPU-Xtal & Straps
54	GPU-BUFFER PARTITION A/B
55	GDDR6 256Mx2Chx16bit _ChA
56	GDDR6 256Mx2Chx16bit _ChB
57	GPU-BUFFER PARTITION C/D
58	GDDR6 256Mx2Chx16bit _ChC
59	GDDR6 256Mx2Chx16bit _ChD
60	HDMI/mDP Conn
61	GPU HDMI/mDP
62	GPU-GPIO
63	GPU-POWER&GND
64	GPU-Decoupling
65	GPU_MIO
66	GPU_IFPAB_DDI

67	GPU_POWER Sequence	88	GPU_POWER_CAP
68	DC_IN	89	GPU POWER DISCHARGE
69	Charger	90	Power Sense
70	VR CONTROLLER	91	+12V_FAN
71-72	Vcore Driver	92	
73	Vccgt Driver	93	CARD-USB CON
74	Vccsa Driver		
75	Vcore & VccGT CAP		
76	+1P05VSB/+2P5VVP		
77	+1P2V_DUAL & +VTDDR		
78	+3VA / +5VA		
79	+VCCIO / +1P8VSB		
80-81	Load switch		
82	NVVDD CONTROLLER		
83-84	NVVDD Driver		
85			
86	+FBVDDQ		
87	+1P0V_GPU/+1P8V_GPU & LDO		

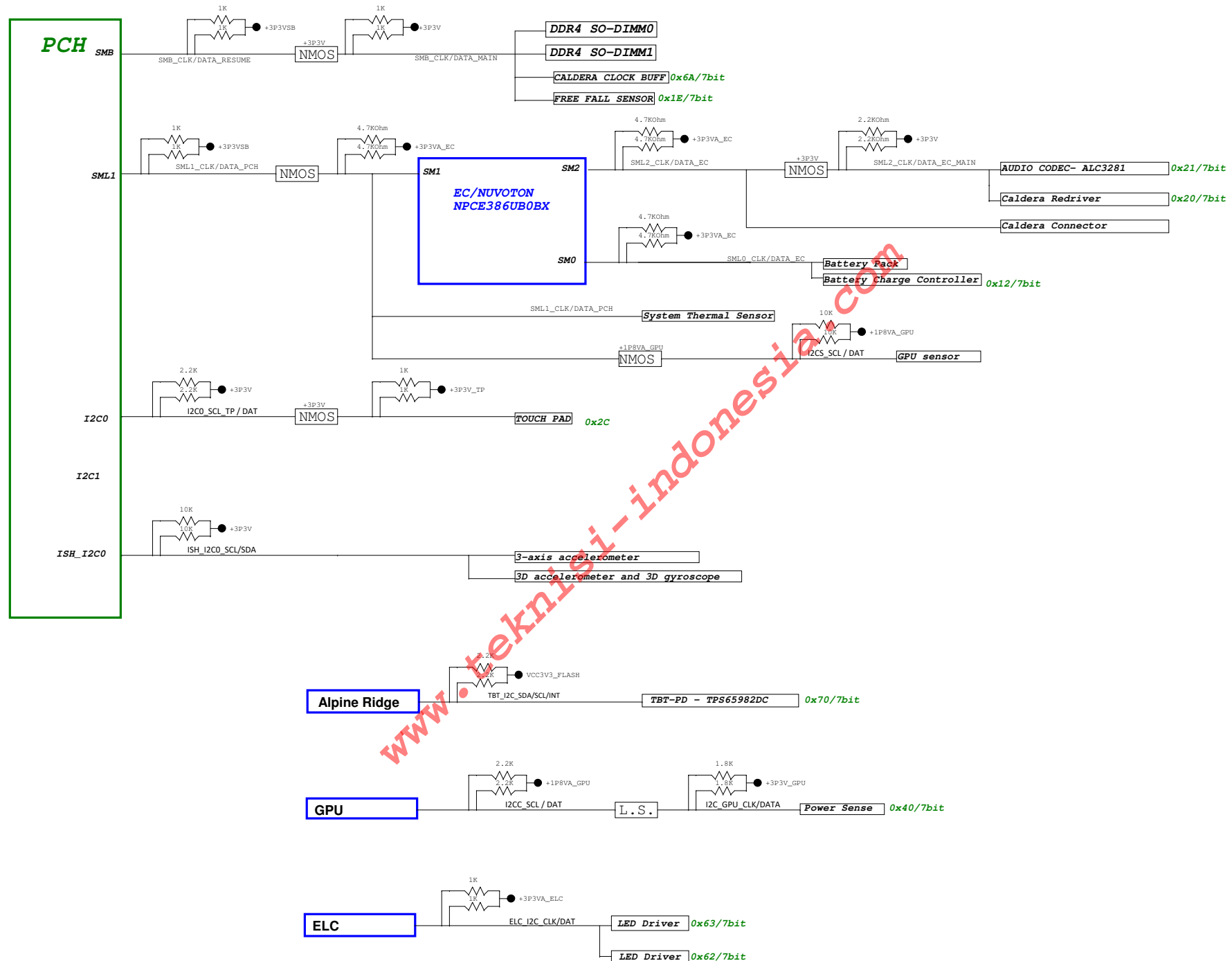
Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

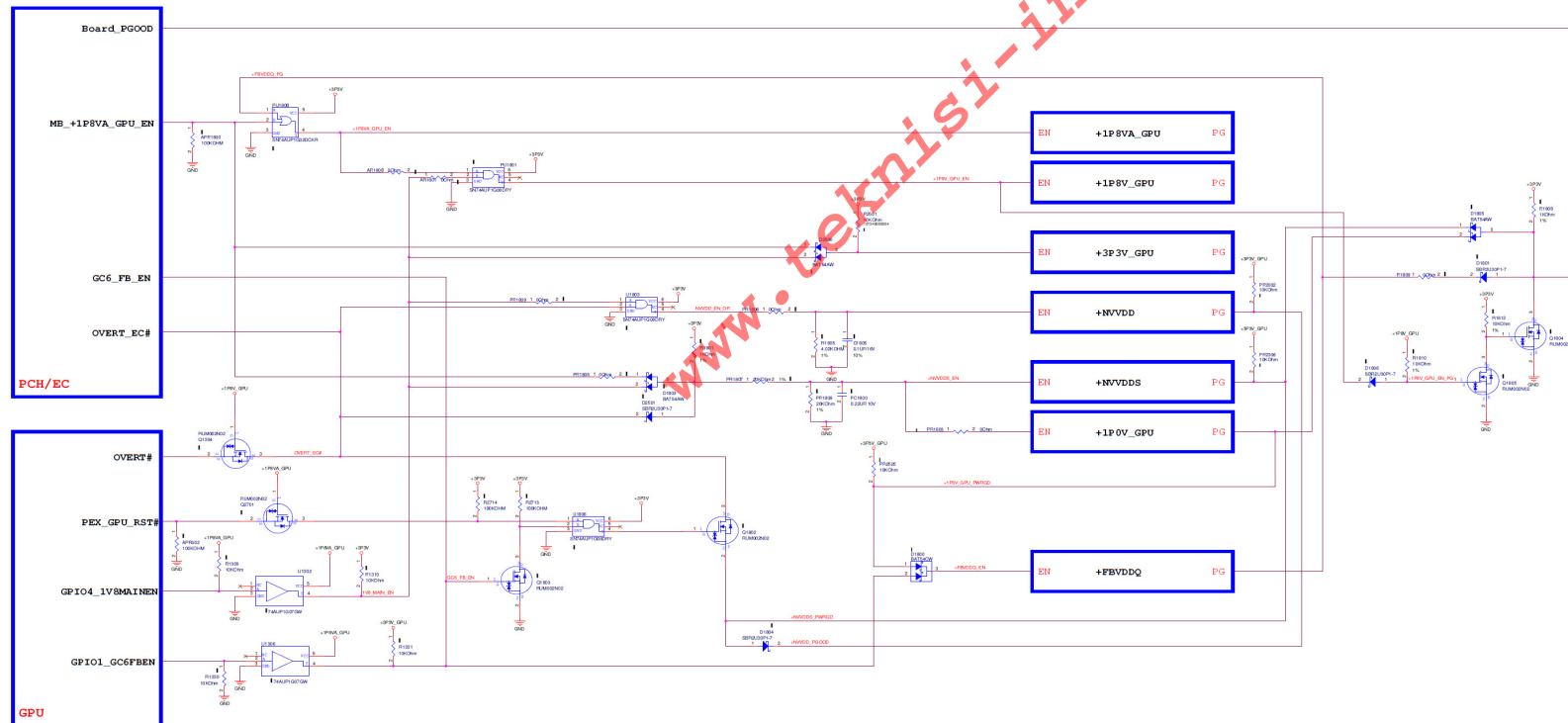
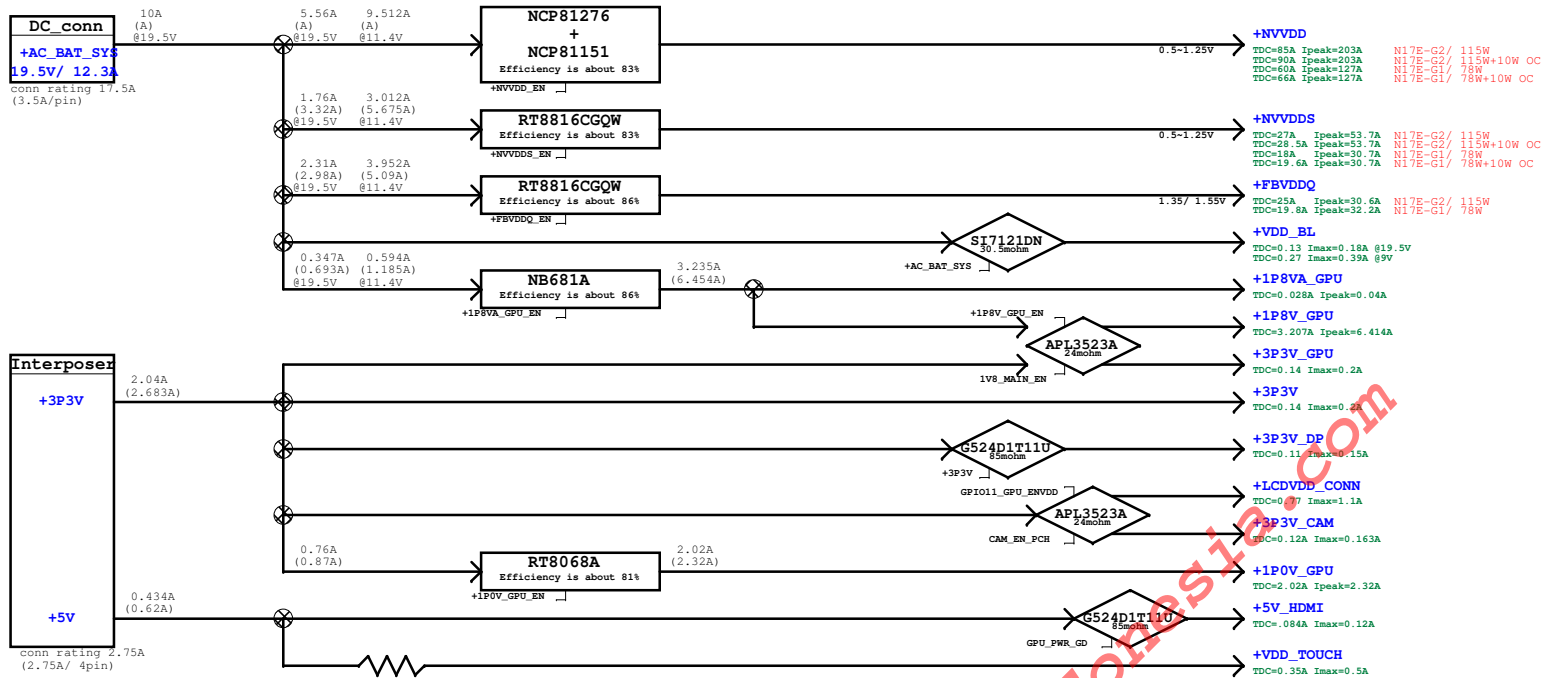
Property: BOM
I = Installed Part.
NI = Not Installed Part.
PROTO = PROTO Phase Only.
VP = Virtual Part.



[illegible]

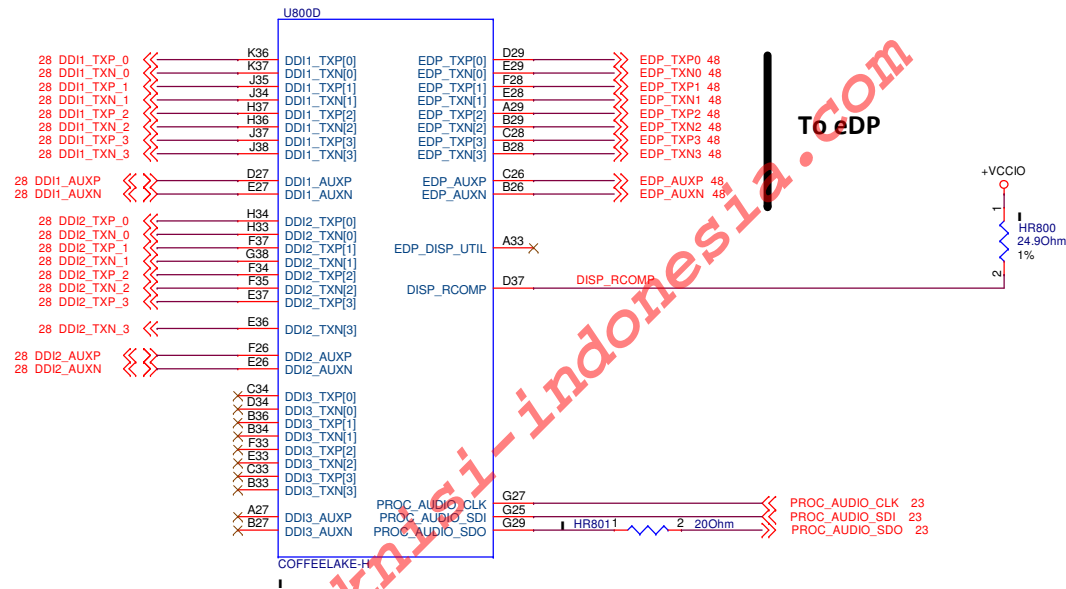
SMBUS & I2C Block Diagram





www.teknisi-indonesia.com

To Apline ridge



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU DD/EDP

Pegatron Corp. Engineer: Ryan_Yen

Size A3 Project Name Orion_N18E Rev A00

Date: Friday, December 14, 2018 Sheet 8 of 93

18 M_CHB_DQ[0..63]



SODIMM

RCOMP [0]	M	MS	VSS	2	12-15				20	25/25			500	121
RCOMP [1]	M	MS	VSS	2	12-15				20	25/25			500	75
RCOMP [2]	M	MS	VSS	2	12-15				20	25/25			500	100

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU DDR4 CHB

Pegatron Corp. Engineer: Ryan_Yen

Size A3 Project Name Orion_N18E

Date: Friday, December 14, 2018 Sheet 10 of 93

Caldera x 4

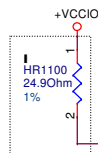
Alpine Ridge x 4

GPU x 8

Caldera x 4

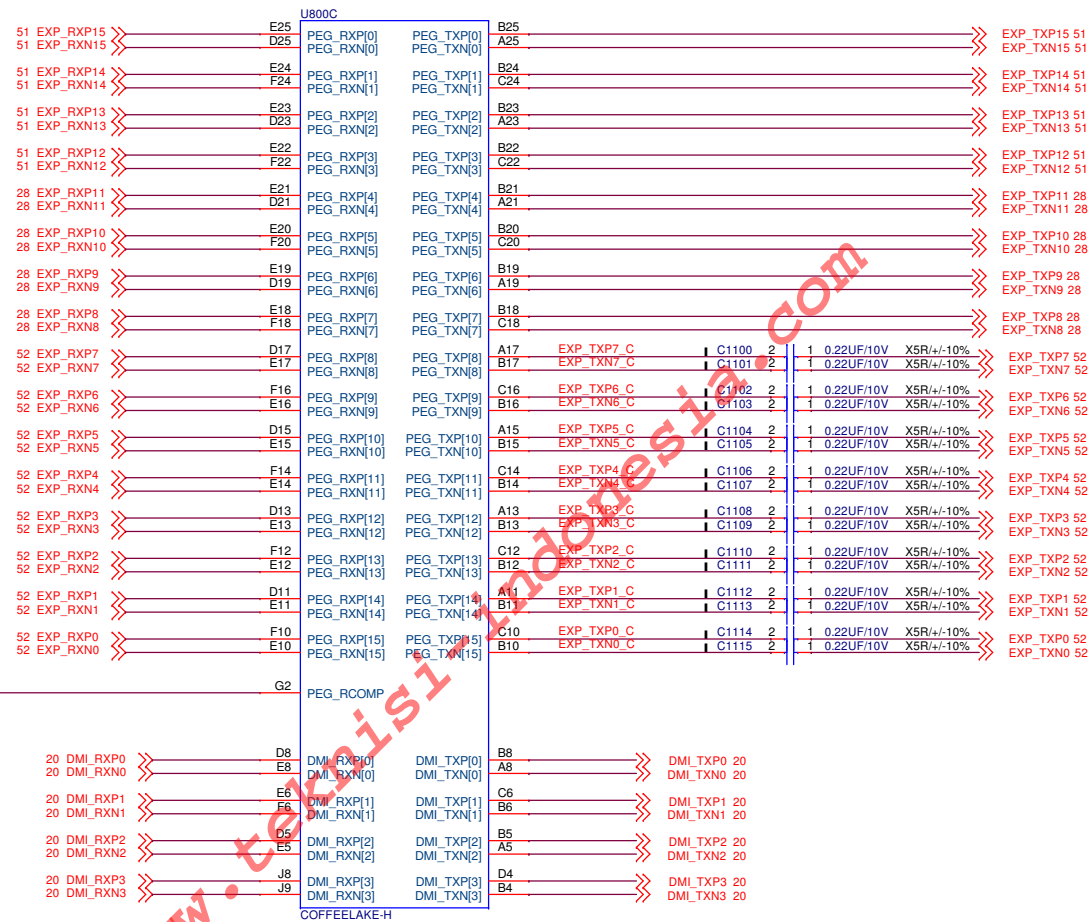
Alpine Ridge x 4

GPU x 8



NOTE:

W/S=12/15 mil, length<400mil



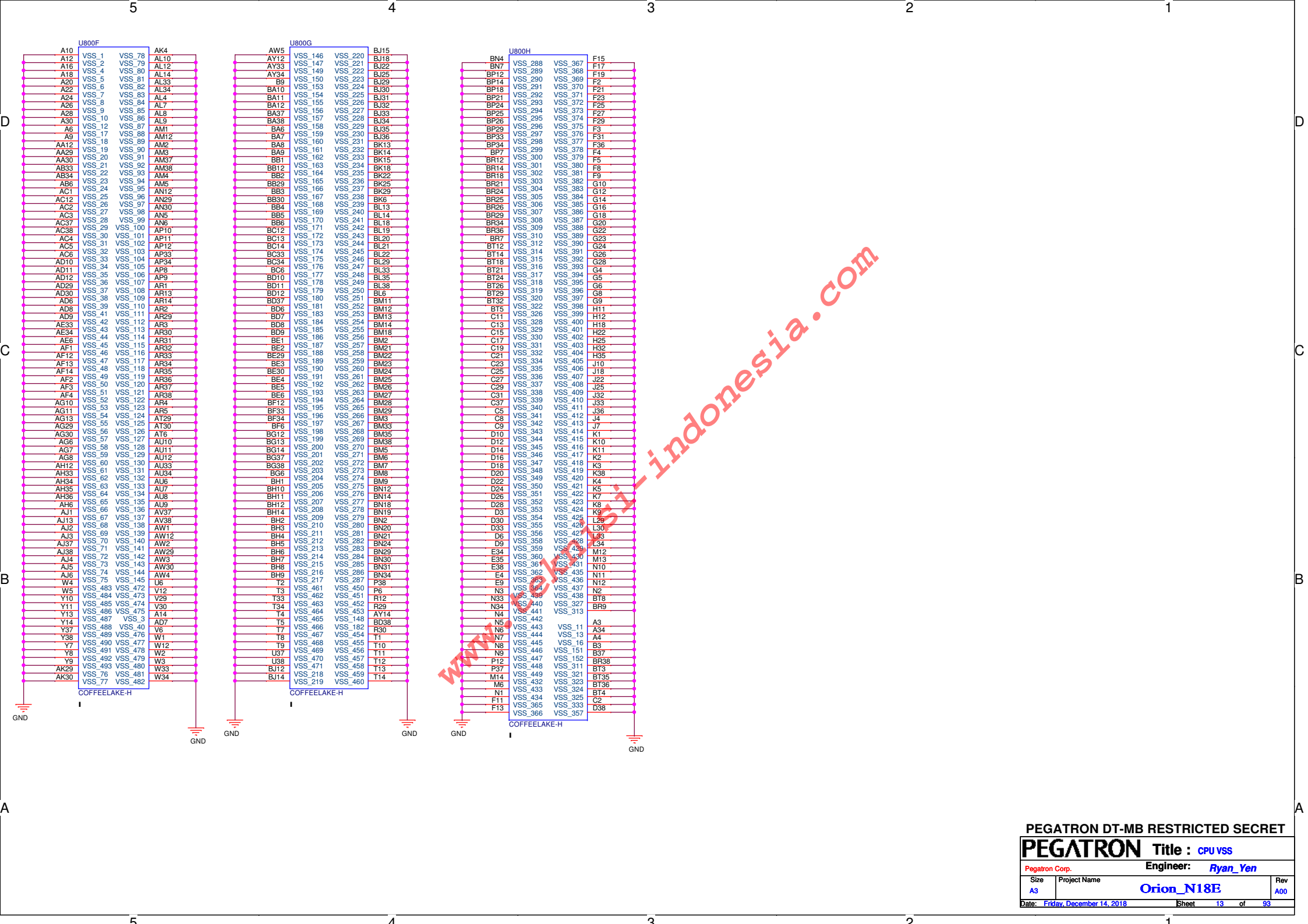
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU PCIE/DMI

Pegatron Corp. Engineer: Ryan_Yen

Size A3 Project Name Orion_N18E Rev A00

Date: Friday, December 14, 2018 Sheet 11 of 93



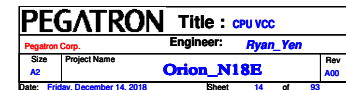
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU VSS

Pegatron Corp. Engineer: **Ryan_Yen**

Size A3	Project Name Orion_N18E	Rev A00
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Date: **Friday, December 14, 2018** Sheet **13** of **93**



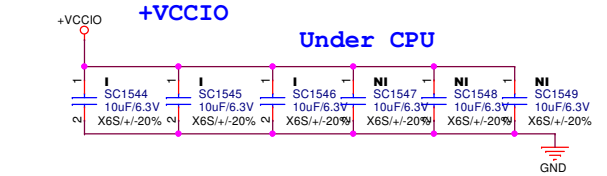
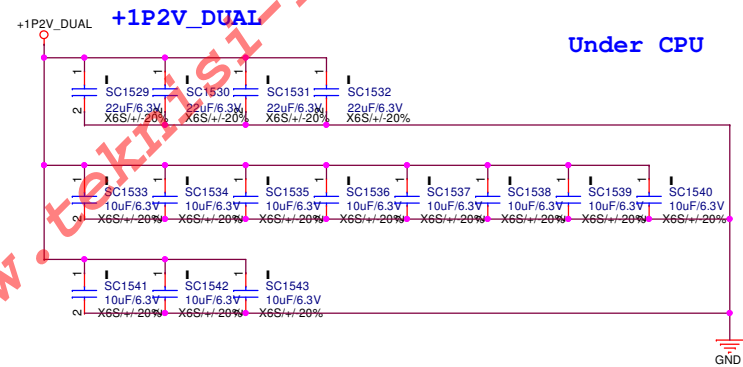
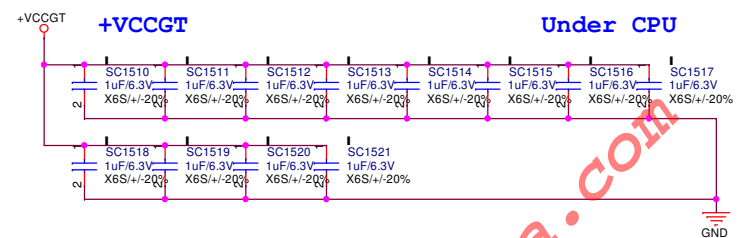
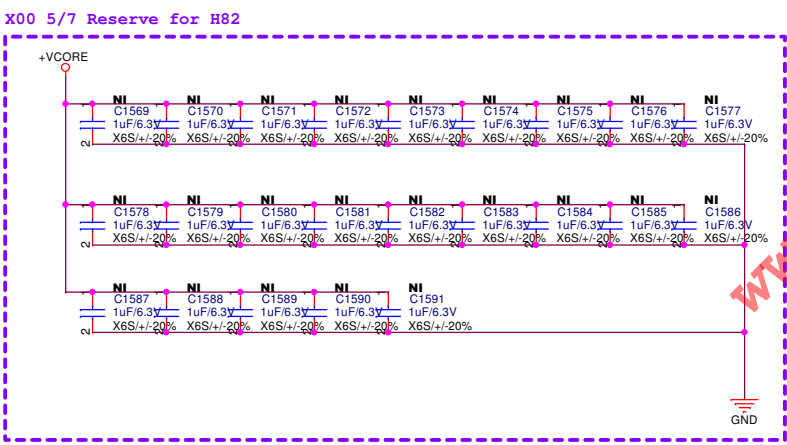
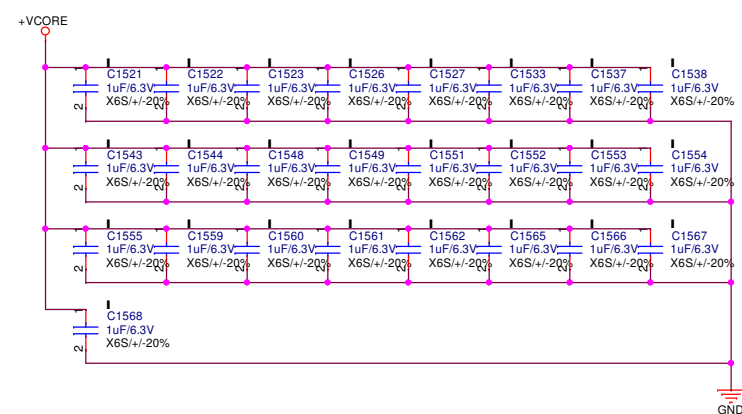
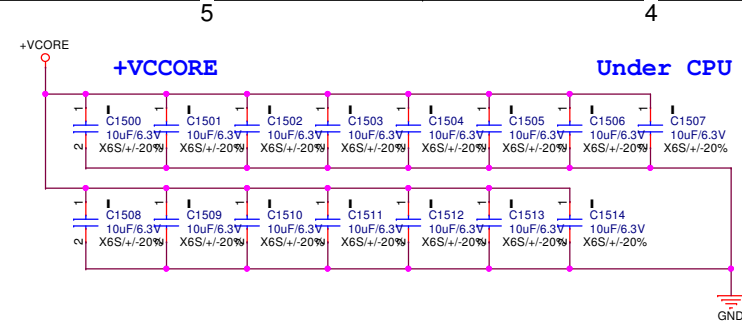
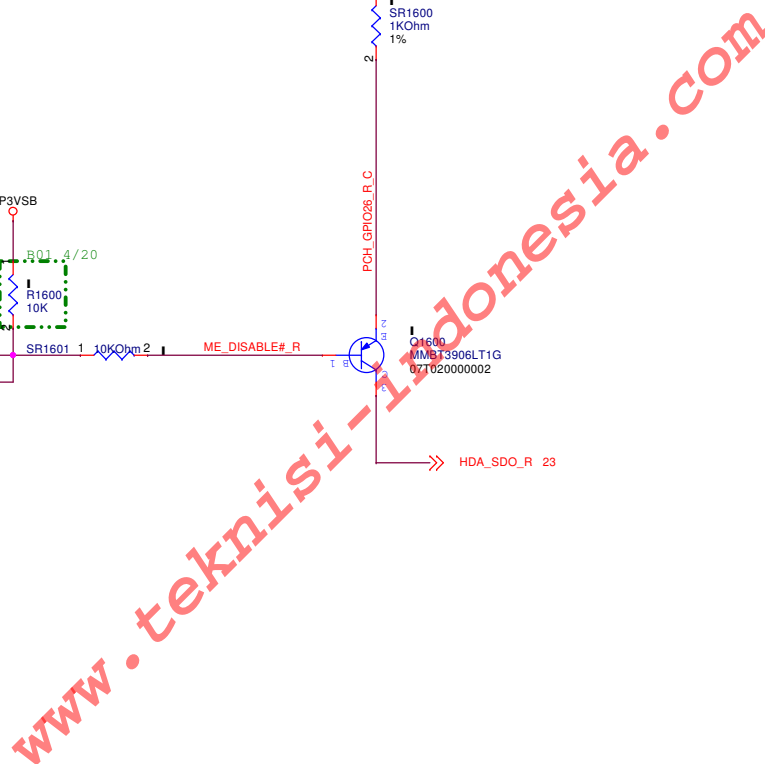
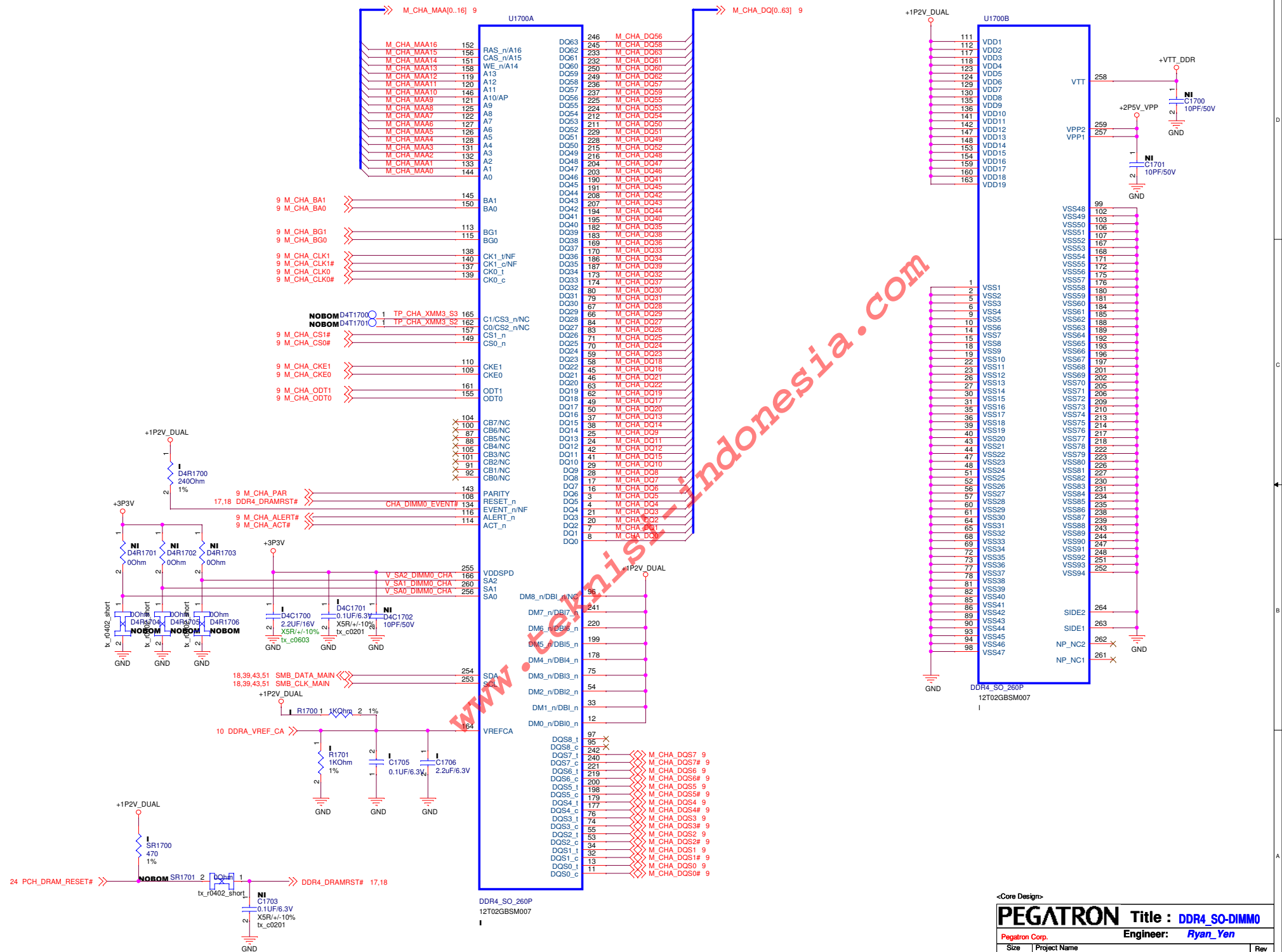


Table 50-3. Decoupling Requirements for CFL H Processor

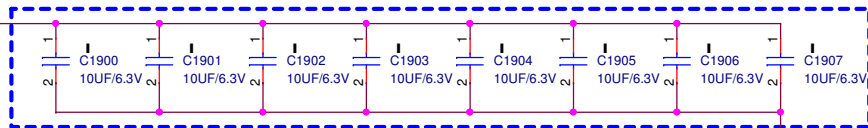
Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805	12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
VccGT	3x 47uF 0805 7x 22uF 0603		Place as close to the BGA as possible
		10x 10uF 0402	
		12x 1uF 0201	
VccSA	2x 47uF 0805 2x 22uF 0603		
		7x 10uF 0402 1x 1uF 0201	
VDDQ		4x 22uF 0603 11x 10uF 0402	
		3x 10uF 0402	
VCCIO		3x 0402 (placeholder)	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.



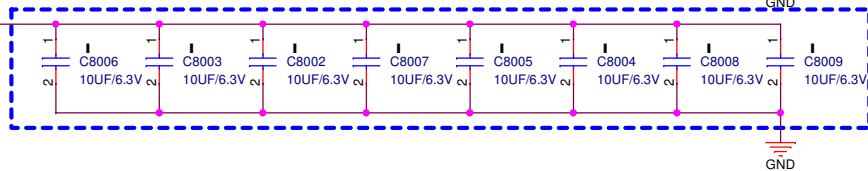
PEGATRON		Title : ME disable	
Pegatron Corp.		Engineer: Ryan_Yen	
Size A3	Project Name Orion_N18E	Rev A00	
Date: Friday, December 14, 2018		Sheet	16 of 93



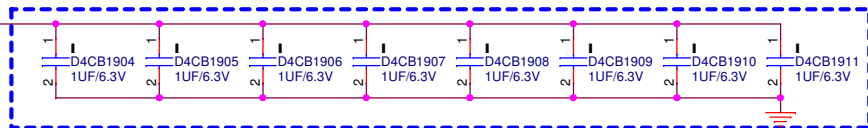
+1P2V_DUAL



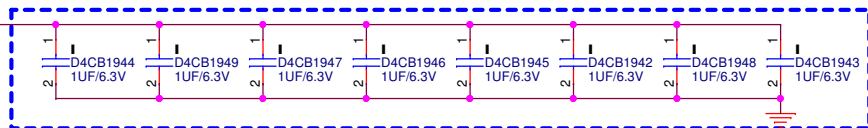
close
CH A SO-DIMM



close
CH B SO-DIMM



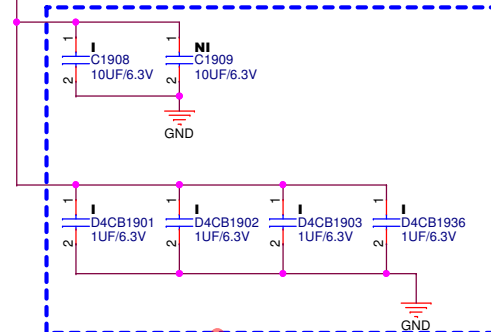
close
CH A SO-DIMM



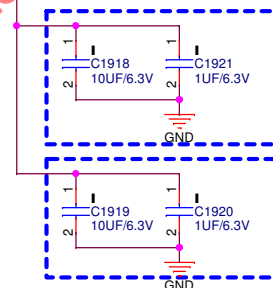
close
CH B SO-DIMM

+VTT_DDR

Near SO-DIMM



+2P5V_VPP



close CH A SO-DIMM

close CH B SO-DIMM

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 2.2µF (0402)	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : DDR4 DECOUPLING	
Pegatron Corp.		Engineer: Ryan_Yen	
Size Custom	Project Name Orion_N18E	Rev A00	
Date: Friday, December 14, 2018		Sheet	19 of 93

(LAN) Killer NIC

M.2 KEY-E WLAN

HDD

M.2 PCIE X4 #2

PCIE/SATA

C38 PCIE13_TXP/SATA0B_TXP
C39 PCIE13_TXN/SATA0B_TXN
C40 PCIE13_RXP/SATA0B_RXP
C41 PCIE13_RXN/SATA0B_RXN

C42 PCIE14_TXP/SATA1B_TXP
C43 PCIE14_TXN/SATA1B_TXN
C44 PCIE14_RXP/SATA1B_RXP
C45 PCIE14_RXN/SATA1B_RXN

C46 PCIE15_TXP/SATA2_TXP
C47 PCIE15_TXN/SATA2_TXN
C48 PCIE15_RXP/SATA2_RXP
C49 PCIE15_RXN/SATA2_RXN

C50 PCIE16_TXP/SATA3_TXP
C51 PCIE16_TXN/SATA3_TXN
C52 PCIE16_RXP/SATA3_RXP
C53 PCIE16_RXN/SATA3_RXN

C54 PCIE17_TXP/SATA4_TXP
C55 PCIE17_TXN/SATA4_TXN
C56 PCIE17_RXP/SATA4_RXP
C57 PCIE17_RXN/SATA4_RXN

C58 PCIE18_TXP/SATA5_TXP
C59 PCIE18_TXN/SATA5_TXN
C60 PCIE18_RXP/SATA5_RXP
C61 PCIE18_RXN/SATA5_RXN

C62 PCIE19_TXP/SATA6_TXP
C63 PCIE19_TXN/SATA6_TXN
C64 PCIE19_RXP/SATA6_RXP
C65 PCIE19_RXN/SATA6_RXN

C66 PCIE20_TXP/SATA7_TXP
C67 PCIE20_TXN/SATA7_TXN
C68 PCIE20_RXP/SATA7_RXP
C69 PCIE20_RXN/SATA7_RXN

C70 PCIE21_TXP
C71 PCIE21_TXN
C72 PCIE21_RXP
C73 PCIE21_RXN

C74 PCIE22_TXP
C75 PCIE22_TXN
C76 PCIE22_RXP
C77 PCIE22_RXN

C78 PCIE23_TXP
C79 PCIE23_TXN
C80 PCIE23_RXP
C81 PCIE23_RXN

C82 PCIE24_TXP
C83 PCIE24_TXN
C84 PCIE24_RXP
C85 PCIE24_RXN

C86 PCIE21_SSD2_TXP
C87 PCIE21_SSD2_TXN
C88 PCIE21_SSD2_RXP
C89 PCIE21_SSD2_RXN

C90 PCIE22_SSD2_TXP
C91 PCIE22_SSD2_TXN
C92 PCIE22_SSD2_RXP
C93 PCIE22_SSD2_RXN

C94 PCIE23_SSD2_TXP
C95 PCIE23_SSD2_TXN
C96 PCIE23_SSD2_RXP
C97 PCIE23_SSD2_RXN

C98 PCIE24_SSD2_TXP
C99 PCIE24_SSD2_TXN
C100 PCIE24_SSD2_RXP
C101 PCIE24_SSD2_RXN

C102 PCIE21_TXP
C103 PCIE21_TXN
C104 PCIE21_RXP
C105 PCIE21_RXN

C106 PCIE22_TXP
C107 PCIE22_TXN
C108 PCIE22_RXP
C109 PCIE22_RXN

C110 PCIE23_TXP
C111 PCIE23_TXN
C112 PCIE23_RXP
C113 PCIE23_RXN

C114 PCIE24_TXP
C115 PCIE24_TXN
C116 PCIE24_RXP
C117 PCIE24_RXN

C118 PCIE21_SSD2_TXP
C119 PCIE21_SSD2_TXN
C120 PCIE21_SSD2_RXP
C121 PCIE21_SSD2_RXN

C122 PCIE22_SSD2_TXP
C123 PCIE22_SSD2_TXN
C124 PCIE22_SSD2_RXP
C125 PCIE22_SSD2_RXN

C126 PCIE23_SSD2_TXP
C127 PCIE23_SSD2_TXN
C128 PCIE23_SSD2_RXP
C129 PCIE23_SSD2_RXN

C130 PCIE24_SSD2_TXP
C131 PCIE24_SSD2_TXN
C132 PCIE24_SSD2_RXP
C133 PCIE24_SSD2_RXN

C134 PCIE21_TXP
C135 PCIE21_TXN
C136 PCIE21_RXP
C137 PCIE21_RXN

C138 PCIE22_TXP
C139 PCIE22_TXN
C140 PCIE22_RXP
C141 PCIE22_RXN

C142 PCIE23_TXP
C143 PCIE23_TXN
C144 PCIE23_RXP
C145 PCIE23_RXN

C146 PCIE24_TXP
C147 PCIE24_TXN
C148 PCIE24_RXP
C149 PCIE24_RXN

C150 PCIE21_SSD2_TXP
C151 PCIE21_SSD2_TXN
C152 PCIE21_SSD2_RXP
C153 PCIE21_SSD2_RXN

C154 PCIE22_SSD2_TXP
C155 PCIE22_SSD2_TXN
C156 PCIE22_SSD2_RXP
C157 PCIE22_SSD2_RXN

C158 PCIE23_SSD2_TXP
C159 PCIE23_SSD2_TXN
C160 PCIE23_SSD2_RXP
C161 PCIE23_SSD2_RXN

C162 PCIE24_SSD2_TXP
C163 PCIE24_SSD2_TXN
C164 PCIE24_SSD2_RXP
C165 PCIE24_SSD2_RXN

C166 PCIE21_TXP
C167 PCIE21_TXN
C168 PCIE21_RXP
C169 PCIE21_RXN

C170 PCIE22_TXP
C171 PCIE22_TXN
C172 PCIE22_RXP
C173 PCIE22_RXN

C174 PCIE23_TXP
C175 PCIE23_TXN
C176 PCIE23_RXP
C177 PCIE23_RXN

C178 PCIE24_TXP
C179 PCIE24_TXN
C180 PCIE24_RXP
C181 PCIE24_RXN

C182 PCIE21_SSD2_TXP
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C184 PCIE21_SSD2_RXP
C185 PCIE21_SSD2_RXN

C186 PCIE22_SSD2_TXP
C187 PCIE22_SSD2_TXN
C188 PCIE22_SSD2_RXP
C189 PCIE22_SSD2_RXN

C190 PCIE23_SSD2_TXP
C191 PCIE23_SSD2_TXN
C192 PCIE23_SSD2_RXP
C193 PCIE23_SSD2_RXN

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C196 PCIE24_SSD2_RXP
C197 PCIE24_SSD2_RXN

C198 PCIE21_TXP
C199 PCIE21_TXN
C200 PCIE21_RXP
C201 PCIE21_RXN

C202 PCIE22_TXP
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C204 PCIE22_RXP
C205 PCIE22_RXN

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C207 PCIE23_TXN
C208 PCIE23_RXP
C209 PCIE23_RXN

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C211 PCIE24_TXN
C212 PCIE24_RXP
C213 PCIE24_RXN

C214 PCIE21_SSD2_TXP
C215 PCIE21_SSD2_TXN
C216 PCIE21_SSD2_RXP
C217 PCIE21_SSD2_RXN

C218 PCIE22_SSD2_TXP
C219 PCIE22_SSD2_TXN
C220 PCIE22_SSD2_RXP
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C229 PCIE24_SSD2_RXN

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C233 PCIE21_RXN

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C236 PCIE22_RXP
C237 PCIE22_RXN

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C239 PCIE23_TXN
C240 PCIE23_RXP
C241 PCIE23_RXN

C242 PCIE24_TXP
C243 PCIE24_TXN
C244 PCIE24_RXP
C245 PCIE24_RXN

C246 PCIE21_SSD2_TXP
C247 PCIE21_SSD2_TXN
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C260 PCIE24_SSD2_RXP
C261 PCIE24_SSD2_RXN

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C263 PCIE21_TXN
C264 PCIE21_RXP
C265 PCIE21_RXN

C266 PCIE22_TXP
C267 PCIE22_TXN
C268 PCIE22_RXP
C269 PCIE22_RXN

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C272 PCIE23_RXP
C273 PCIE23_RXN

C274 PCIE24_TXP
C275 PCIE24_TXN
C276 PCIE24_RXP
C277 PCIE24_RXN

C278 PCIE21_SSD2_TXP
C279 PCIE21_SSD2_TXN
C280 PCIE21_SSD2_RXP
C281 PCIE21_SSD2_RXN

C282 PCIE22_SSD2_TXP
C283 PCIE22_SSD2_TXN
C284 PCIE22_SSD2_RXP
C285 PCIE22_SSD2_RXN

C286 PCIE23_SSD2_TXP
C287 PCIE23_SSD2_TXN
C288 PCIE23_SSD2_RXP
C289 PCIE23_SSD2_RXN

C290 PCIE24_SSD2_TXP
C291 PCIE24_SSD2_TXN
C292 PCIE24_SSD2_RXP
C293 PCIE24_SSD2_RXN

C294 PCIE21_TXP
C295 PCIE21_TXN
C296 PCIE21_RXP
C297 PCIE21_RXN

C298 PCIE22_TXP
C299 PCIE22_TXN
C300 PCIE22_RXP
C301 PCIE22_RXN

C302 PCIE23_TXP
C303 PCIE23_TXN
C304 PCIE23_RXP
C305 PCIE23_RXN

C306 PCIE24_TXP
C307 PCIE24_TXN
C308 PCIE24_RXP
C309 PCIE24_RXN

C310 PCIE21_SSD2_TXP
C311 PCIE21_SSD2_TXN
C312 PCIE21_SSD2_RXP
C313 PCIE21_SSD2_RXN

C314 PCIE22_SSD2_TXP
C315 PCIE22_SSD2_TXN
C316 PCIE22_SSD2_RXP
C317 PCIE22_SSD2_RXN

C318 PCIE23_SSD2_TXP
C319 PCIE23_SSD2_TXN
C320 PCIE23_SSD2_RXP
C321 PCIE23_SSD2_RXN

C322 PCIE24_SSD2_TXP
C323 PCIE24_SSD2_TXN
C324 PCIE24_SSD2_RXP
C325 PCIE24_SSD2_RXN

C326 PCIE21_TXP
C327 PCIE21_TXN
C328 PCIE21_RXP
C329 PCIE21_RXN

C330 PCIE22_TXP
C331 PCIE22_TXN
C332 PCIE22_RXP
C333 PCIE22_RXN

C334 PCIE23_TXP
C335 PCIE23_TXN
C336 PCIE23_RXP
C337 PCIE23_RXN

C338 PCIE24_TXP
C339 PCIE24_TXN
C340 PCIE24_RXP
C341 PCIE24_RXN

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C344 PCIE21_SSD2_RXP
C345 PCIE21_SSD2_RXN

C346 PCIE22_SSD2_TXP
C347 PCIE22_SSD2_TXN
C348 PCIE22_SSD2_RXP
C349 PCIE22_SSD2_RXN

C350 PCIE23_SSD2_TXP
C351 PCIE23_SSD2_TXN
C352 PCIE23_SSD2_RXP
C353 PCIE23_SSD2_RXN

C354 PCIE24_SSD2_TXP
C355 PCIE24_SSD2_TXN
C356 PCIE24_SSD2_RXP
C357 PCIE24_SSD2_RXN

C358 PCIE21_TXP
C359 PCIE21_TXN
C360 PCIE21_RXP
C361 PCIE21_RXN

C362 PCIE22_TXP
C363 PCIE22_TXN
C364 PCIE22_RXP
C365 PCIE22_RXN

C366 PCIE23_TXP
C367 PCIE23_TXN
C368 PCIE23_RXP
C369 PCIE23_RXN

C370 PCIE24_TXP
C371 PCIE24_TXN
C372 PCIE24_RXP
C373 PCIE24_RXN

C374 PCIE21_SSD2_TXP
C375 PCIE21_SSD2_TXN
C376 PCIE21_SSD2_RXP
C377 PCIE21_SSD2_RXN

C378 PCIE22_SSD2_TXP
C379 PCIE22_SSD2_TXN
C380 PCIE22_SSD2_RXP
C381 PCIE22_SSD2_RXN

C382 PCIE23_SSD2_TXP
C383 PCIE23_SSD2_TXN
C384 PCIE23_SSD2_RXP
C385 PCIE23_SSD2_RXN

C386 PCIE24_SSD2_TXP
C387 PCIE24_SSD2_TXN
C388 PCIE24_SSD2_RXP
C389 PCIE24_SSD2_RXN

C390 PCIE21_TXP
C391 PCIE21_TXN
C392 PCIE21_RXP
C393 PCIE21_RXN

C394 PCIE22_TXP
C395 PCIE22_TXN
C396 PCIE22_RXP
C397 PCIE22_RXN

C398 PCIE23_TXP
C399 PCIE23_TXN
C400 PCIE23_RXP
C401 PCIE23_RXN

C402 PCIE24_TXP
C403 PCIE24_TXN
C404 PCIE24_RXP
C405 PCIE24_RXN

C406 PCIE21_SSD2_TXP
C407 PCIE21_SSD2_TXN
C408 PCIE21_SSD2_RXP
C409 PCIE21_SSD2_RXN

C410 PCIE22_SSD2_TXP
C411 PCIE22_SSD2_TXN
C412 PCIE22_SSD2_RXP
C413 PCIE22_SSD2_RXN

C414 PCIE23_SSD2_TXP
C415 PCIE23_SSD2_TXN
C416 PCIE23_SSD2_RXP
C417 PCIE23_SSD2_RXN

C418 PCIE24_SSD2_TXP
C419 PCIE24_SSD2_TXN
C420 PCIE24_SSD2_RXP
C421 PCIE24_SSD2_RXN

C422 PCIE21_TXP
C423 PCIE21_TXN
C424 PCIE21_RXP
C425 PCIE21_RXN

C426 PCIE22_TXP
C427 PCIE22_TXN
C428 PCIE22_RXP
C429 PCIE22_RXN

C430 PCIE23_TXP
C431 PCIE23_TXN
C432 PCIE23_RXP
C433 PCIE23_RXN

C434 PCIE24_TXP
C435 PCIE24_TXN
C436 PCIE24_RXP
C437 PCIE24_RXN

C438 PCIE21_SSD2_TXP
C439 PCIE21_SSD2_TXN
C440 PCIE21_SSD2_RXP
C441 PCIE21_SSD2_RXN

C442 PCIE22_SSD2_TXP
C443 PCIE22_SSD2_TXN
C444 PCIE22_SSD2_RXP
C445 PCIE22_SSD2_RXN

C446 PCIE23_SSD2_TXP
C447 PCIE23_SSD2_TXN
C448 PCIE23_SSD2_RXP
C449 PCIE23_SSD2_RXN

C450 PCIE24_SSD2_TXP
C451 PCIE24_SSD2_TXN
C452 PCIE24_SSD2_RXP
C453 PCIE24_SSD2_RXN

C454 PCIE21_TXP
C455 PCIE21_TXN
C456 PCIE21_RXP
C457 PCIE21_RXN

C458 PCIE22_TXP
C459 PCIE22_TXN
C460 PCIE22_RXP
C461 PCIE22_RXN

C462 PCIE23_TXP
C463 PCIE23_TXN
C464 PCIE23_RXP
C465 PCIE23_RXN

C466 PCIE24_TXP
C467 PCIE24_TXN
C468 PCIE24_RXP
C469 PCIE24_RXN

C470 PCIE21_SSD2_TXP
C471 PCIE21_SSD2_TXN
C472 PCIE21_SSD2_RXP
C473 PCIE21_SSD2_RXN

C474 PCIE22_SSD2_TXP
C475 PCIE22_SSD2_TXN
C476 PCIE22_SSD2_RXP
C477 PCIE22_SSD2_RXN

C478 PCIE23_SSD2_TXP
C479 PCIE23_SSD2_TXN
C480 PCIE23_SSD2_RXP
C481 PCIE23_SSD2_RXN

C482 PCIE24_SSD2_TXP
C483 PCIE24_SSD2_TXN
C484 PCIE24_SSD2_RXP
C485 PCIE24_SSD2_RXN

C486 PCIE21_TXP
C487 PCIE21_TXN
C488 PCIE21_RXP
C489 PCIE21_RXN

C490 PCIE22_TXP
C491 PCIE22_TXN
C492 PCIE22_RXP
C493 PCIE22_RXN

C494 PCIE23_TXP
C495 PCIE23_TXN
C496 PCIE23_RXP
C497 PCIE23_RXN

C498 PCIE24_TXP
C499 PCIE24_TXN
C500 PCIE24_RXP
C501 PCIE24_RXN

C502 PCIE21_SSD2_TXP
C503 PCIE21_SSD2_TXN
C504 PCIE21_SSD2_RXP
C505 PCIE21_SSD2_RXN

C506 PCIE22_SSD2_TXP
C507 PCIE22_SSD2_TXN
C508 PCIE22_SSD2_RXP
C509 PCIE22_SSD2_RXN

C510 PCIE23_SSD2_TXP
C511 PCIE23_SSD2_TXN
C512 PCIE23_SSD2_RXP
C513 PCIE23_SSD2_RXN

C514 PCIE24_SSD2_TXP
C515 PCIE24_SSD2_TXN
C516 PCIE24_SSD2_RXP
C517 PCIE24_SSD2_RXN

C518 PCIE21_TXP
C519 PCIE21_TXN
C520 PCIE21_RXP
C521 PCIE21_RXN

C522 PCIE22_TXP
C523 PCIE22_TXN
C524 PCIE22_RXP
C525 PCIE22_RXN

C526 PCIE23_TXP
C527 PCIE23_TXN
C528 PCIE23_RXP
C529 PCIE23_RXN

C530 PCIE24_TXP
C531 PCIE24_TXN
C532 PCIE24_RXP
C533 PCIE24_RXN

C534 PCIE21_SSD2_TXP
C535 PCIE21_SSD2_TXN
C536 PCIE21_SSD2_RXP
C537 PCIE21_SSD2_RXN

C538 PCIE22_SSD2_TXP
C539 PCIE22_SSD2_TXN
C540 PCIE22_SSD2_RXP
C541 PCIE22_SSD2_RXN

C542 PCIE23_SSD2_TXP
C543 PCIE23_SSD2_TXN
C544 PCIE23_SSD2_RXP
C545 PCIE23_SSD2_RXN

C546 PCIE24_SSD2_TXP
C547 PCIE24_SSD2_TXN
C548 PCIE24_SSD2_RXP
C549 PCIE24_SSD2_RXN

C550 PCIE21_TXP
C551 PCIE21_TXN
C552 PCIE21_RXP
C553 PCIE21_RXN

C554 PCIE22_TXP
C555 PCIE22_TXN
C556 PCIE22_RXP
C557 PCIE22_RXN

C558 PCIE23_TXP
C559 PCIE23_TXN
C560 PCIE23_RXP
C561 PCIE23_RXN

C562 PCIE24_TXP
C563 PCIE24_TXN
C564 PCIE24_RXP
C565 PCIE24_RXN

C566 PCIE21_SSD2_TXP
C567 PCIE21_SSD2_TXN
C568 PCIE21_SSD2_RXP
C569 PCIE21_SSD2_RXN

C570 PCIE22_SSD2_TXP
C571 PCIE22_SSD2_TXN
C572 PCIE22_SSD2_RXP
C573 PCIE22_SSD2_RXN

C574 PCIE23_SSD2_TXP
C575 PCIE23_SSD2_TXN
C576 PCIE23_SSD2_RXP
C577 PCIE23_SSD2_RXN

C578 PCIE24_SSD2_TXP
C579 PCIE24_SSD2_TXN
C580 PCIE24_SSD2_RXP
C581 PCIE24_SSD2_RXN

C582 PCIE21_TXP
C583 PCIE21_TXN
C584 PCIE21_RXP
C585 PCIE21_RXN

C586 PCIE22_TXP
C587 PCIE22_TXN
C588 PCIE22_RXP
C589 PCIE22_RXN

C590 PCIE23_TXP
C591 PCIE23_TXN
C592 PCIE23_RXP
C593 PCIE23_RXN

C594 PCIE24_TXP
C595 PCIE24_TXN
C596 PCIE24_RXP
C597 PCIE24_RXN

C598 PCIE21_SSD2_TXP
C599 PCIE21_SSD2_TXN
C600 PCIE21_SSD2_RXP
C601 PCIE21_SSD2_RXN

C602 PCIE22_SSD2_TXP
C603 PCIE22_SSD2_TXN
C604 PC

NOTE:

eSPI operates at 1.8V

NOTE:

Check SERIRQ & PIRQA volt level

NOTE:

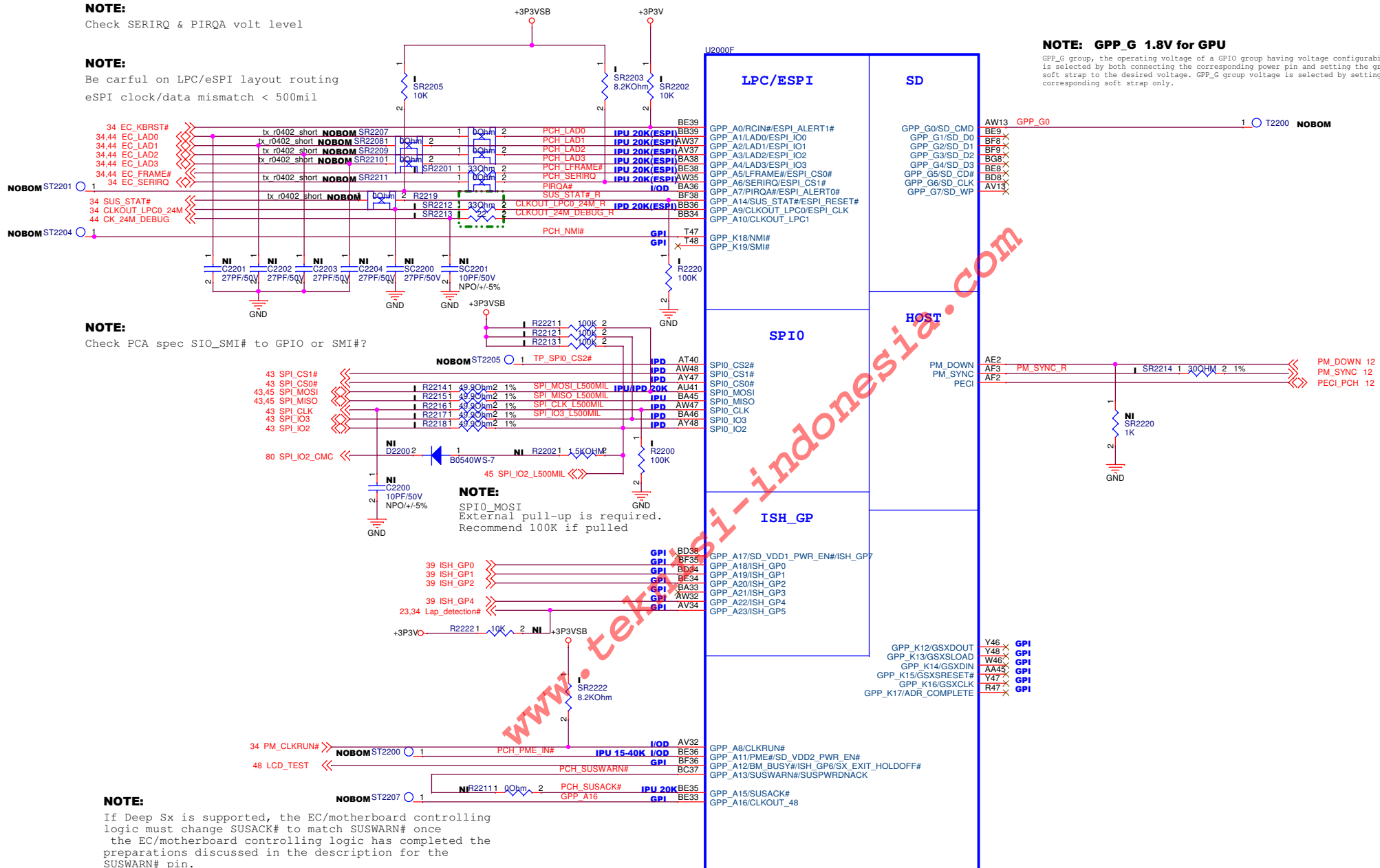
Be careful on LPC/eSPI layout routing
eSPI clock/data mismatch < 500mil

NOTE:

Check GPP_A0 power well

NOTE: GPP_G 1.8V for GPU

GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage selection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **PCH ESPI/SPI/FAN/HOST**

Pegatron Corp.		Engineer: Ryan_Yen	
Size	Project Name	Orion_N18E	
Custom			
Date: Friday, December 14, 2018	Sheet	22	of 93

NOTE:

GPIO_MOSI/GPP_B18

The signal has a weak internal pull-down.

0 = Disable "No Reboot" mode.
1 = Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).

NOTE:

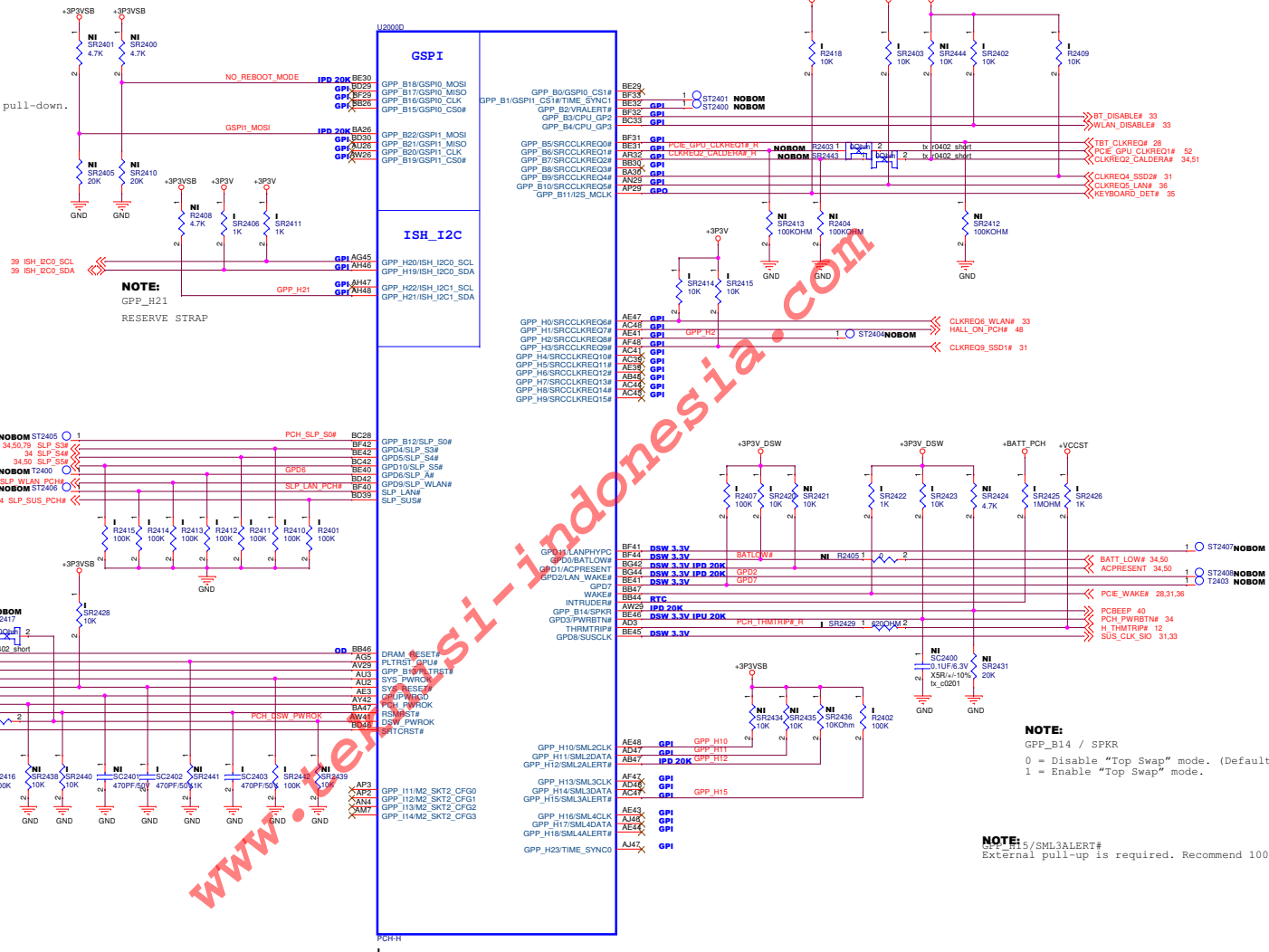
GPP_B22/GSPi1_MOSI

This Signal has a weak internal pull-down.

Offset: 3410h:Bit 10

0: SPI

1: LPC



NOTE:

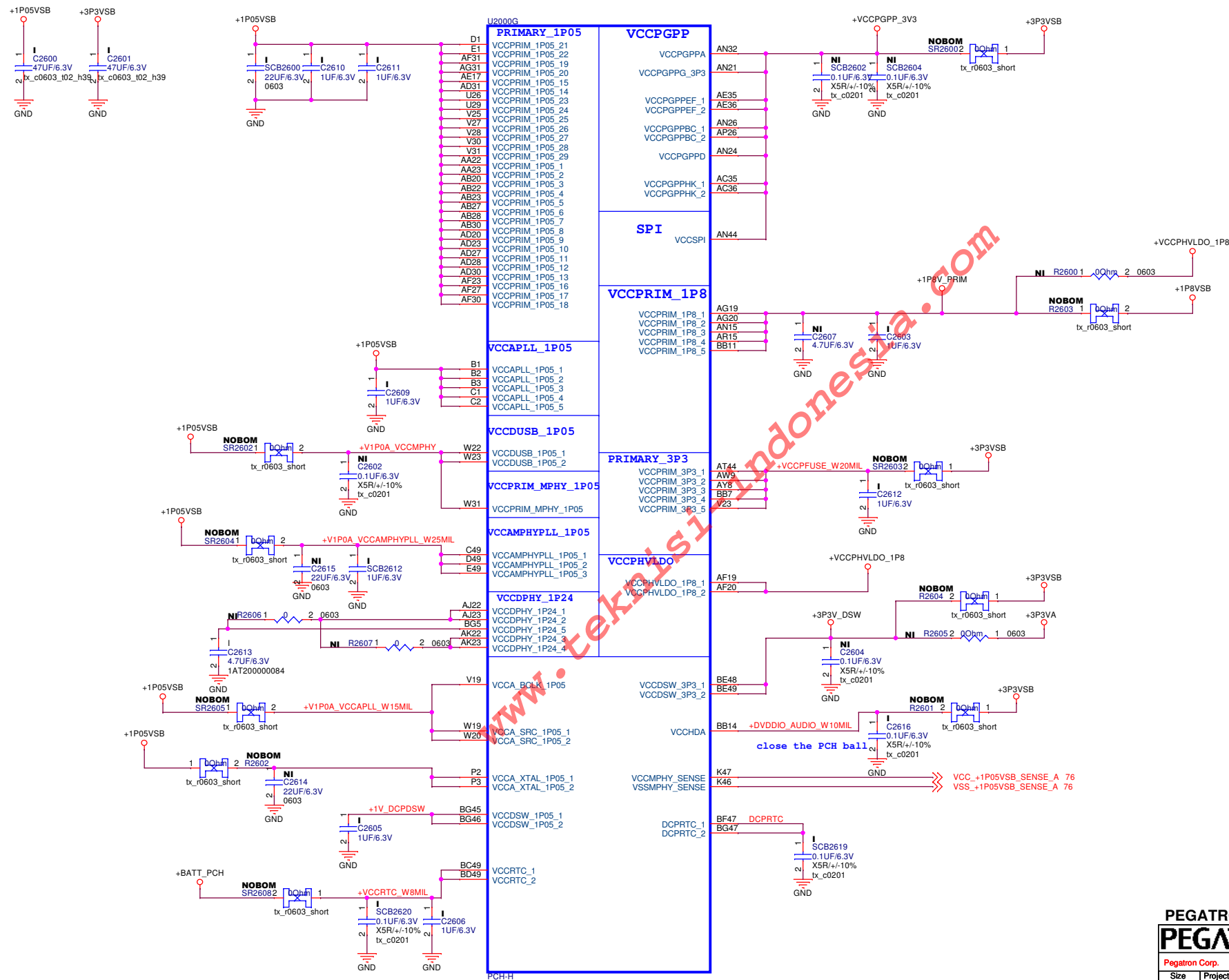
GPP_B14 / SPKR

0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.

NOTE:

GPP_B15/SML3ALERT#

External pull-up is required. Recommend 100K if pulled



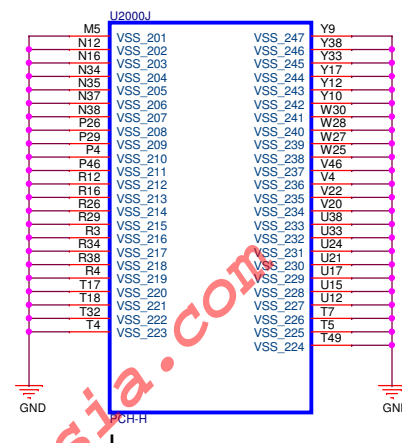
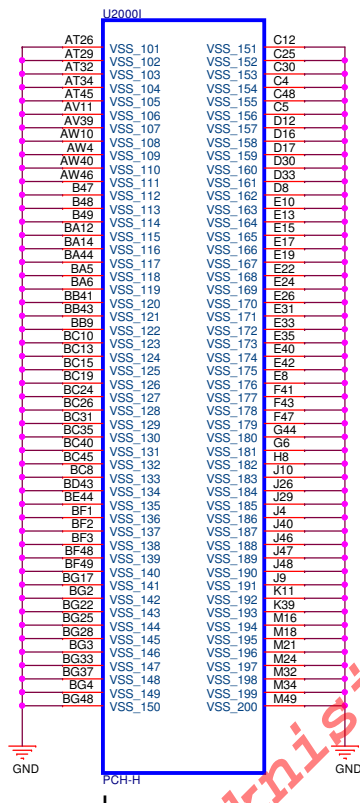
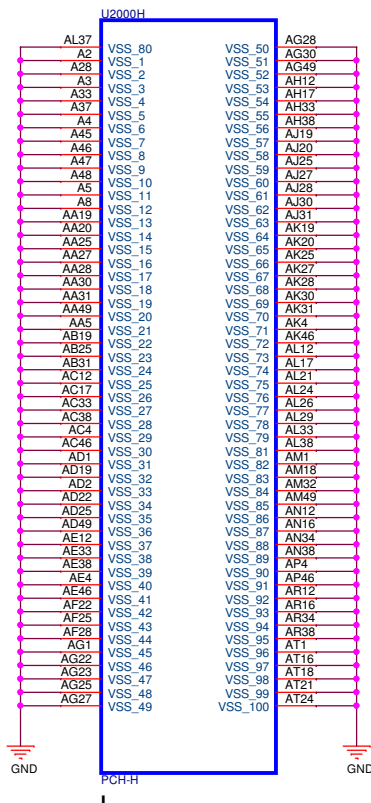
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH VCC/PLL

Pegatron Corp. Engineer: **Ryan_Yen**

Size A3 Project Name **Orion_N18E** Rev A00

Date: Friday, December 14, 2018 Sheet 26 of 93



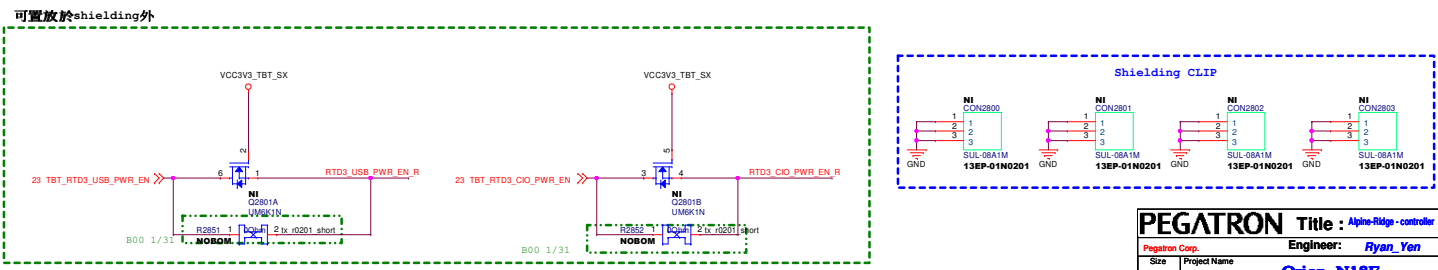
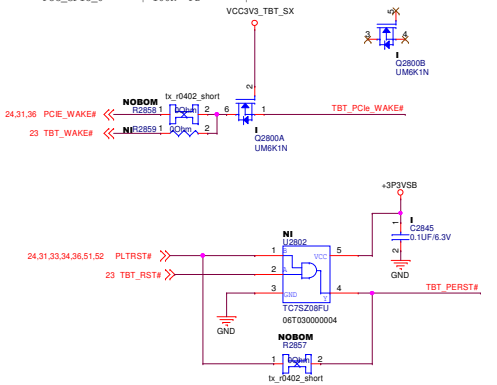
PEGATRON DT-MB RESTRICTED SECRET

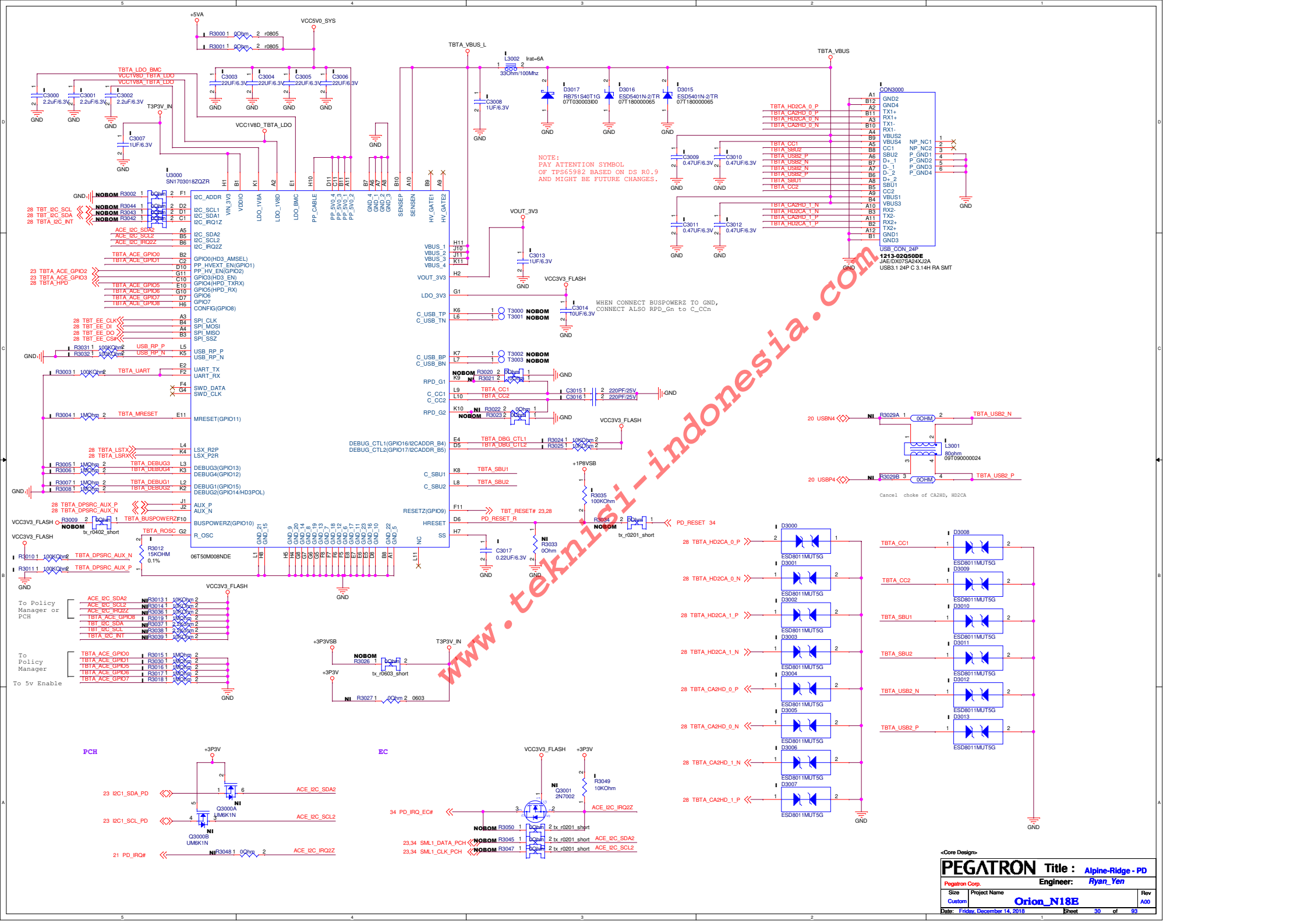
PEGATRON Title : PCH VSS

Pegatron Corp. Engineer: Ryan_Yen

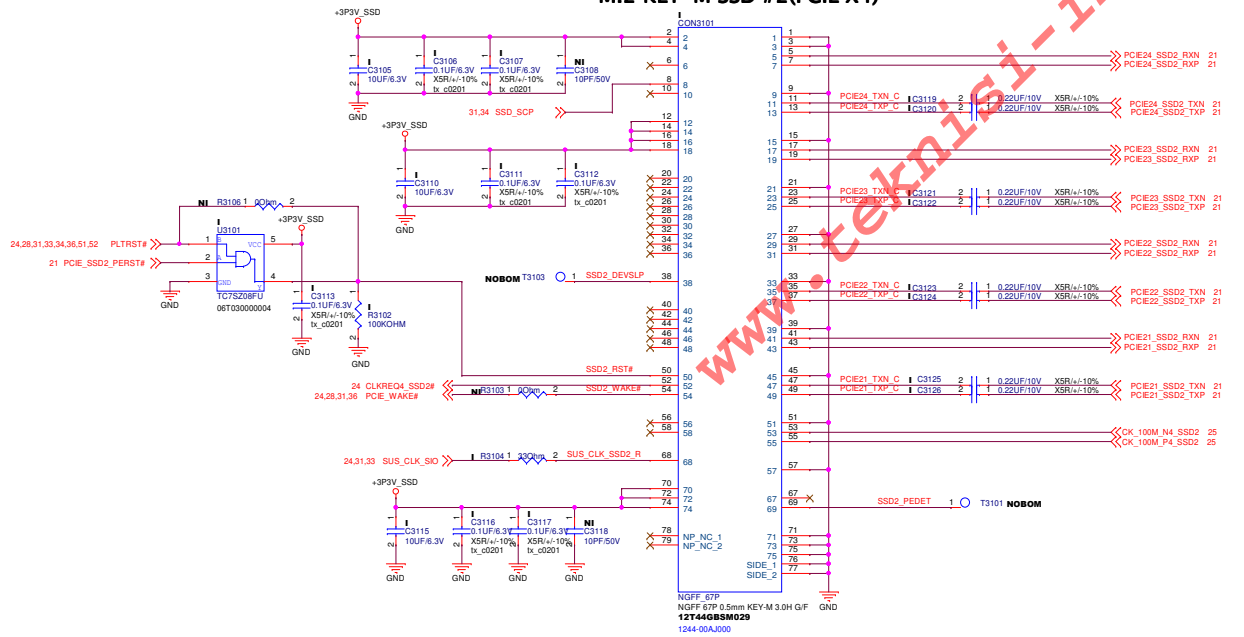
Size A3 Project Name Orion_N18E Rev A00

Date: Friday, December 14, 2018 Sheet 27 of 93

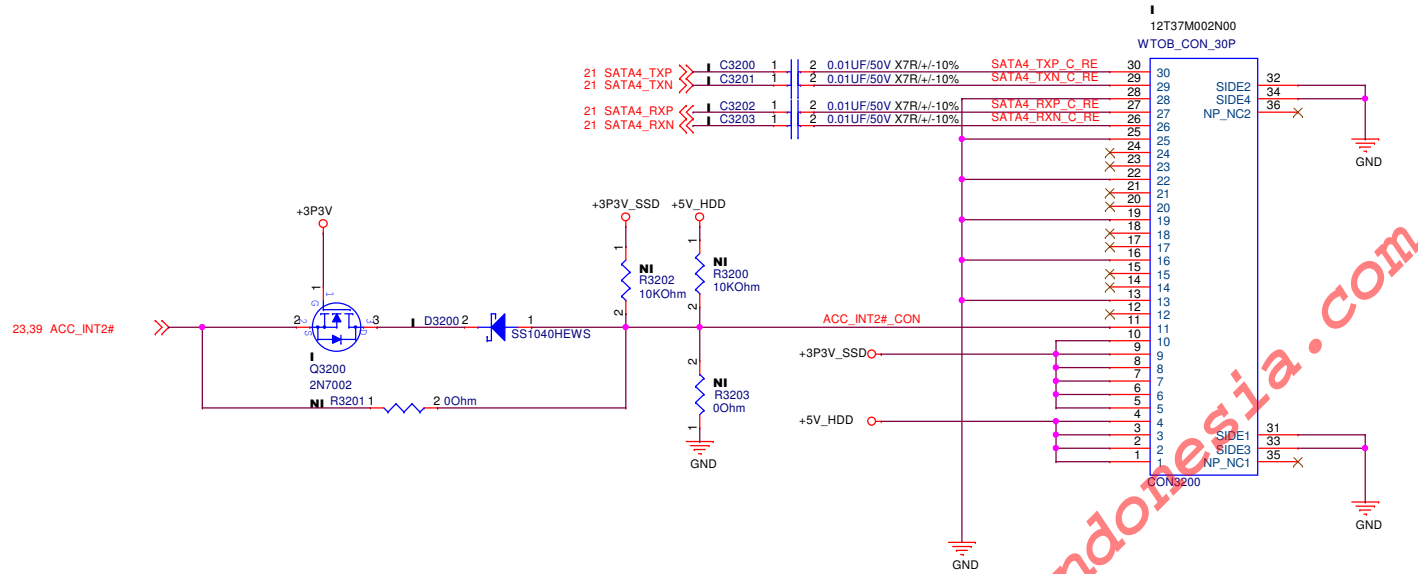




M.2 KEY-M SSD #2(PCIe X4)



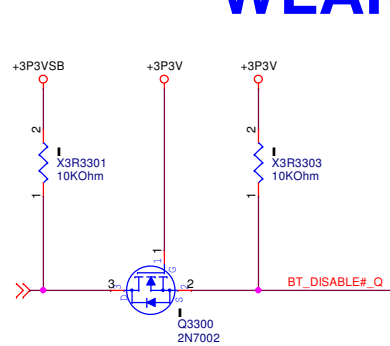
SATA CONN



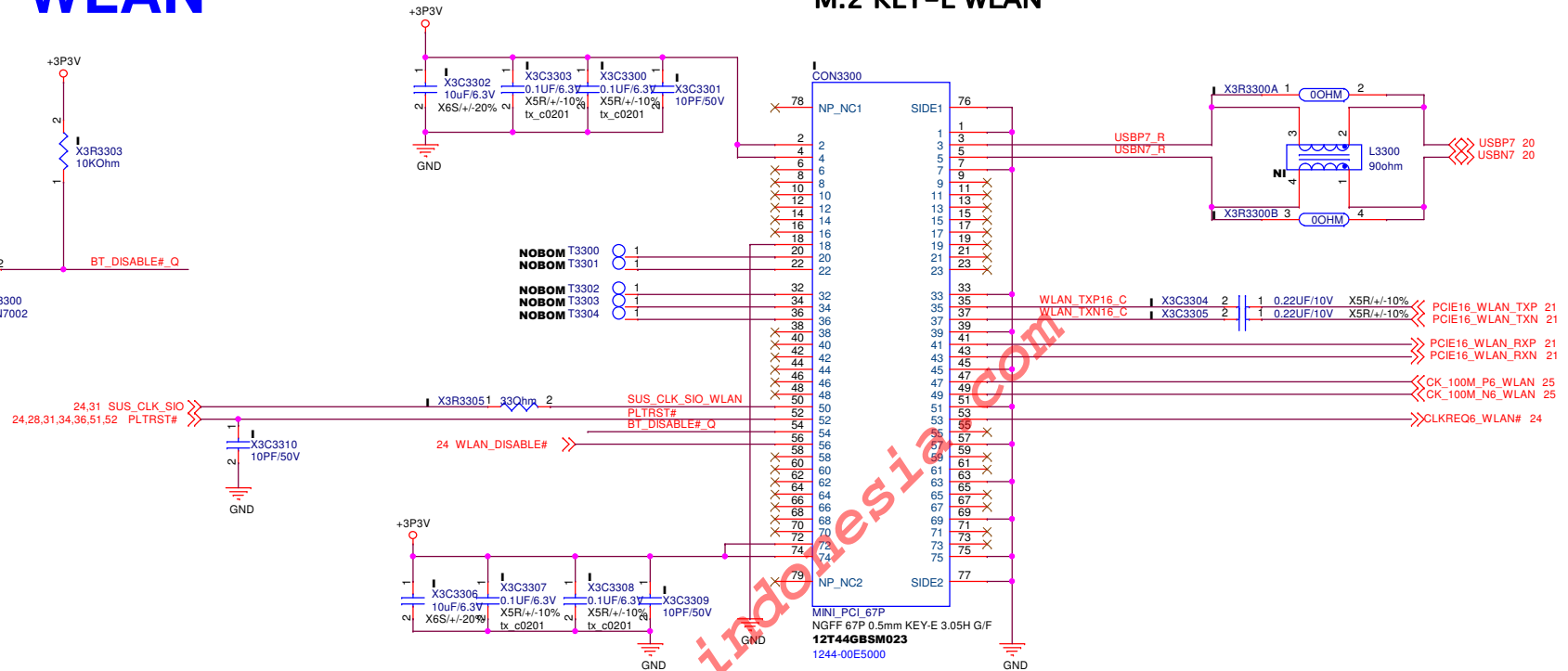
<Core Design>

PEGATRON		Title : SATA HDD	
Pegatron Corp.		Engineer: Ryan_Yen	
Size A3	Project Name Orion_N18E	Rev A00	
Date: Friday, December 14, 2018	Sheet 32	of 93	

WLAN



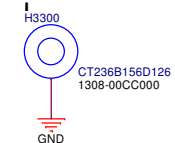
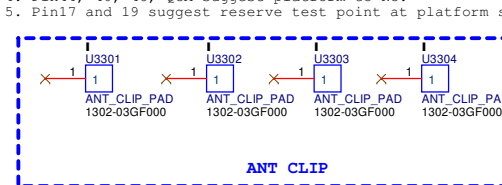
M.2 KEY-E WLAN



59	PERp1	NC	60	I2C_CLK[I]	NC
57	GND	YES	58	I2C_DATA[IO]	NC
55	PCIE_WAKE_L	YES	56	WLAN_DISABLE_L	YES
53	PCIE_CLKREQ_L	YES	54	BT_DISABLE_L	YES
51	GND	YES	52	PCIE_RST_L	YES
49	REFCLKN0	YES	50	SUSCLK(32kHz)	NC(Reverse resister)
47	REFCLKP0	YES	48	LTE_SYNC	YES
45	GND	YES	46	LTE_PRI	YES
43	PETn0	YES	44	LTE_ACTIVE	YES
41	PETp0	YES	42	RSVD	NC
39	GND	YES	40	RSVD	NC
37	PERn0	PCIE_TX_P	38	RSVD	NC
35	PERp0	PCIE_TX_N	36	UART_CTS	YES
33	GND	YES	34	UART_RTS	YES
31	NC	NC	32	UART_RXD	YES
29	NC	NC	30	NC	NC
27	NC	NC	28	NC	NC
25	NC	NC	26	NC	NC
23	NC	NC	24	NC	NC
21	NC	NC	22	UART_TXD	YES
19	DBG_UART_RXD	YES	20	UART_WAKEHOST_L	YES
17	DBG_UART_TXD	YES	18	GND	YES
15	NC	NC	16	LED_BT	YES
13	NC	NC	14	NC	NC
11	NC	NC	12	NC	NC
9	NC	NC	10	NC	NC
7	GND	YES	8	NC	NC
5	USB_D_N	YES	6	LED_WLAN	YES
3	USB_D_P	YES	4	3.3V	YES
1	GND	YES	2	3.3V	YES

Pin #	Name	DUT Connection	Pin #	Name	DUT Connection
75	GND	YES			
73	REFCLKN1	NC	74	3_3V	YES
71	REFCLKP1	NC	72	3_3V	YES
69	GND	YES	70	PEWAKE1	NC
67	PETn1	NC	68	CLKREQ1	NC
65	PETp1	NC	66	PERST1	NC
63	GND	YES	64	RSVD	NC(Reverse resister)
61	PERn1	NC	62	ALERT[0]	NC

- Remark: 1.NC is not connected; YES is connected.
 2. Pin54 is BT_DISABLE_L; Pin56 is WLAN_DISABLE_L.
 3. Pin 20,22,32,34 and 36 are GPIO and have internal pull up(QCA6174A?5), Suggest platform NC those pins.
 4. Pin44, 46, 48, QCA suggest platform to NC.
 5. Pin17 and 19 suggest reserve test point at platform side.



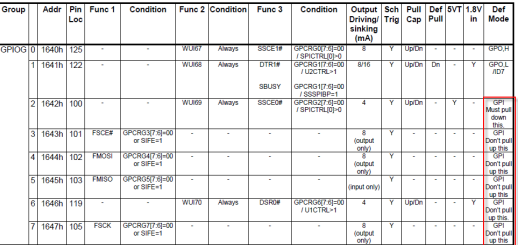
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : M.2 KEY-A 2230 WLAN

Pegatron Corp. Engineer: Ryan_Yen

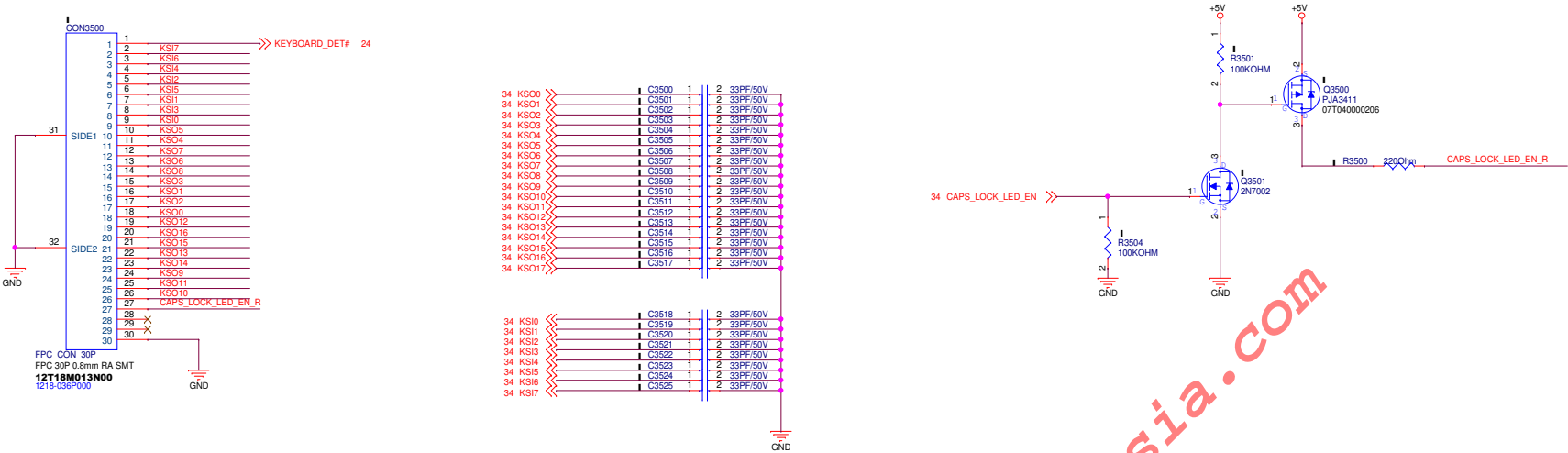
Size A3 Project Name Orion_N18E Rev A00

Date: Friday, December 14, 2018 Sheet 33 of 93



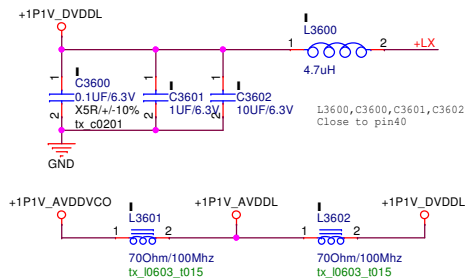
SCP(System Crash Protection)
The SCP Signal is an active low signal,
and it is triggered on negative edge.
The SCP Signal is pulled high at the SSD.

KeyBoard connector

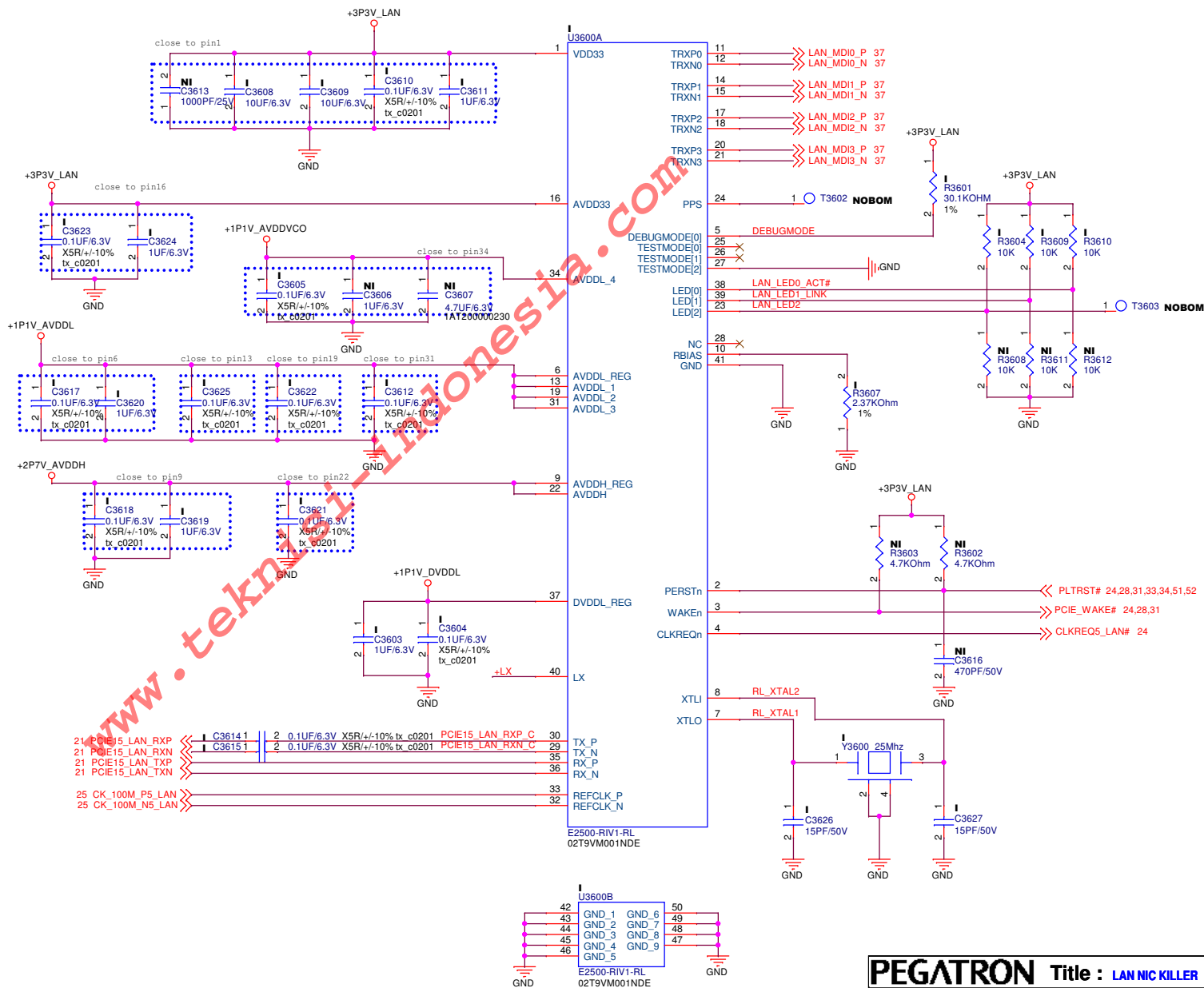


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : KB & NKRO	
Pegatron Corp.		Engineer: Ryan_Yen	
Size	Project Name		Rev
Custom	Orion_N18E		A00
Date: Friday, December 14, 2018		Sheet	35 of 93



**If AVDDL/DVDDL comes from internal SWR: mount L3602;
If AVDDL/DVDDL comes from internal LDO: no mount L3602, L3600, C3600, C3601, C3602

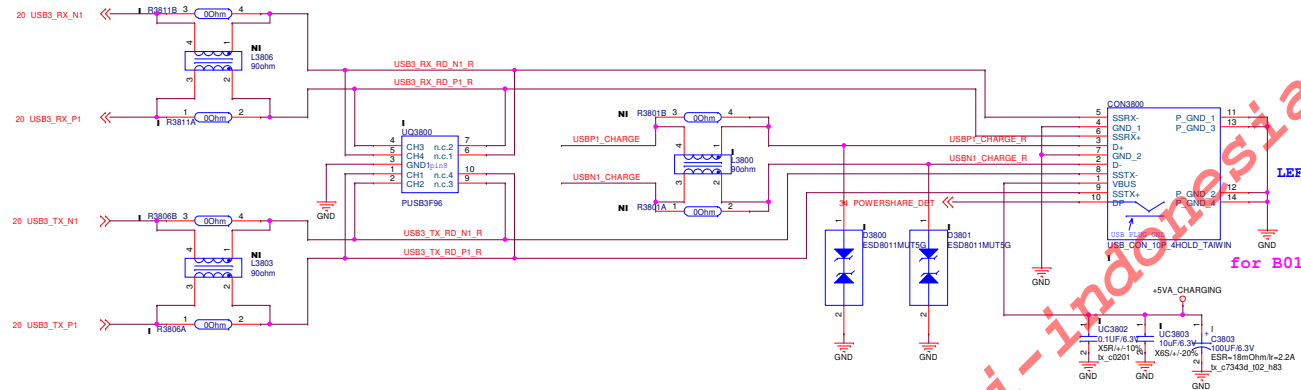


U3600 & U3601 Co-lay
QCA8171-BL3A-R
02T3TM003NDE

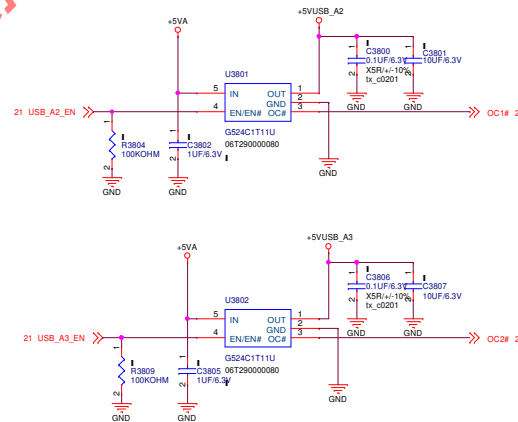
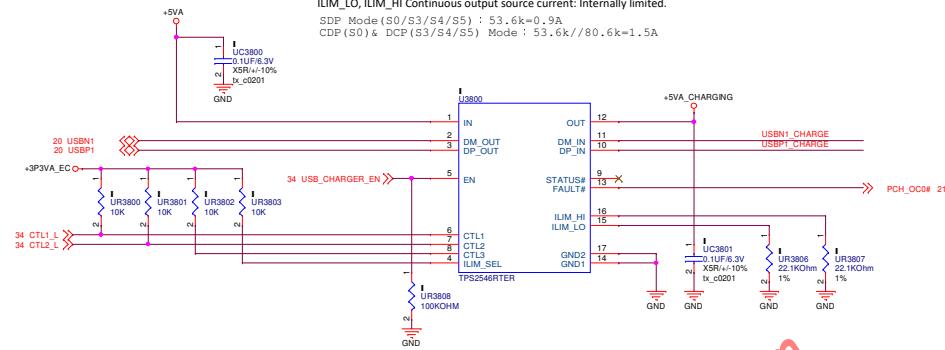
Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	CURRENT LIMIT SETTING	STATUS OUTPUT (Active low)	COMMENT
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	0	1	1	DCP_Auto	I_{OS_PV} & ILIM_HI ⁽¹⁾	DCP load present ⁽²⁾	Data Lines Disconnected and Load Detect Function Active
0	1	0	0	SDP1	ILIM_LO	OFF	Data Lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP load present ⁽³⁾	Data Lines Disconnected and Load Detect Function Active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device Forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	
1	0	1	0	DCP / Divider1	ILIM_LO	OFF	Device Forced to stay in DCP Divider1 Charging Mode
1	0	1	1	DCP / Divider1	ILIM_HI	OFF	
1	1	0	0	SDP1	ILIM_LO	OFF	
1	1	0	1	SDP1	ILIM_HI	OFF	Data Lines Connected
1	1	1	0	SDP2 ⁽⁴⁾	ILIM_LO	OFF	
1	1	1	1	CDP ⁽⁵⁾	ILIM_HI	CDP load present ⁽⁶⁾	Data Lines Connected and Load Detect Active

- (1) TPS2546 : Current limit (I_{OS}) is automatically switched between I_{OS_PV} and the value set by ILIM_HI according to the Load Detect – Power Wake functionality.
(2) DCP Load present governed by the "Load Detection – Power Wake" limits.
(3) DCP Load present governed by the "Load Detection – Non Power Wake" limits.
(4) No OUT discharge when changing between 1111 and 1110.
(5) CDP Load present governed by the "Load Detection – Non Power Wake" limits and BC1.2 primary detection.



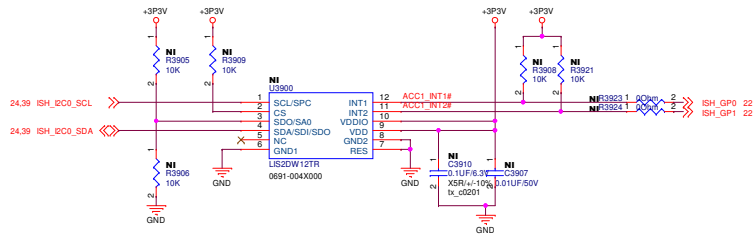
STATUS#, FAULT#, ILIM_LO, ILIM_HI Voltage: 0.3 to 7v.
STATUS#, FAULT# Continuous output sink current: 25mA.
ILIM_LO, ILIM_HI Continuous output source current: Internally limited.
SDP Mode (S0/S3/S4/S5) : 53.6k=0.9A
CDP (S0) & DCP (S3/S4/S5) Mode : 53.6k//80.6k=1.5A



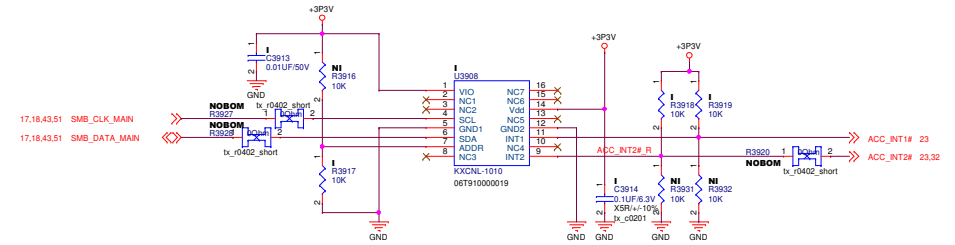
<Core Design>

PEGATRON		Title : USB CONN & POWER	
Pegatron Corp.		Engineer: Ryan_Yen	
Size	Project Name	Rev	
A2	Orion_N18E	A00	
Date: Friday, December 14, 2018		Sheet 38 of 93	

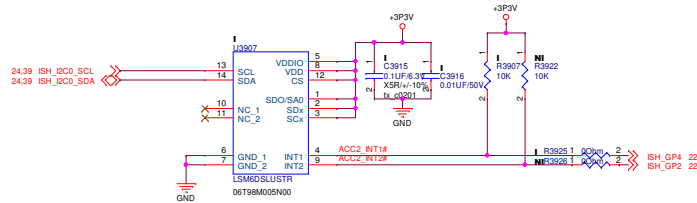
3-axis accelerometer



Free fall sensor

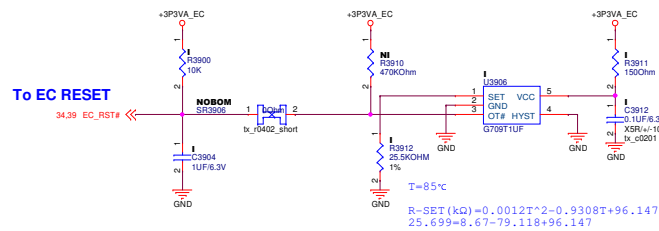


3D accelerometer and 3D gyroscope

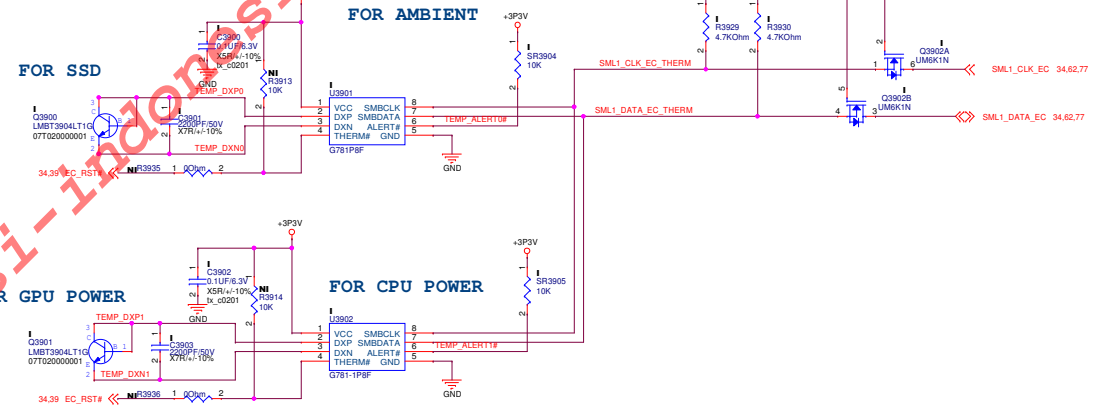
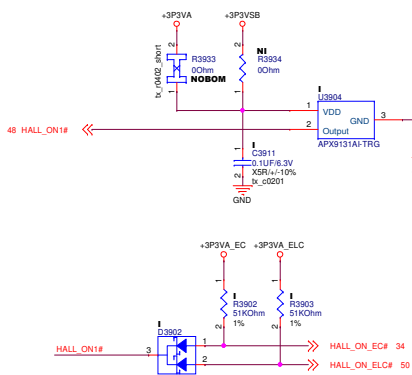


ADDR pin status	SAD	SAD + Read	SAD + Write
ADDR = 0	0011110 (1Eh)	00111101 (3Dh)	00111100 (3Ch)
ADDR = 1	0011101 (1Dh)	00111011 (3Bh)	00111010 (3Ah)

FOR HW thermal protection

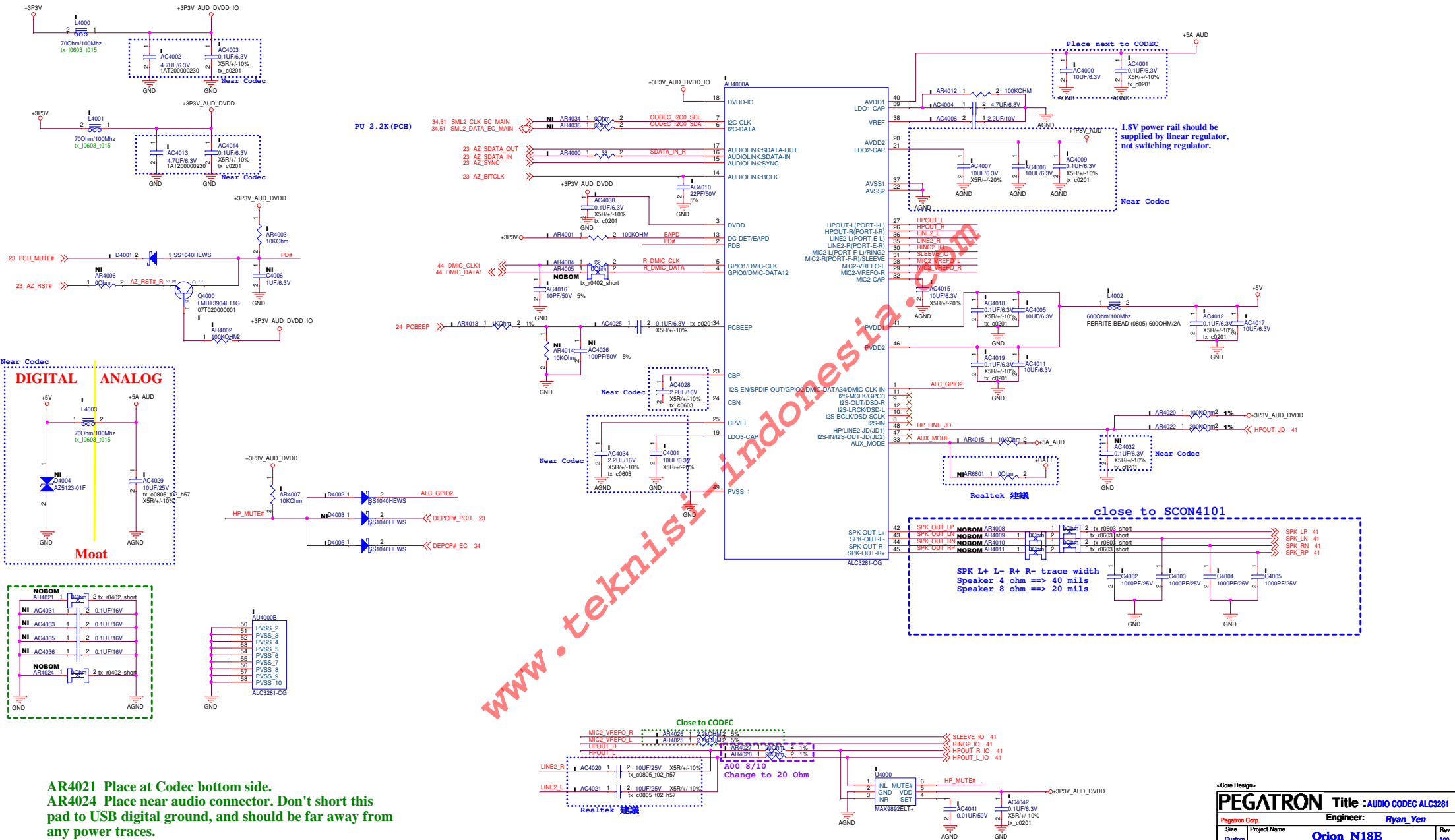


HALL SENSOR



	A6	A5	A4	A3	A2	A1	A0
G781	1	0	0	1	1	0	0
G781-1	1	0	0	1	1	0	1

AUDIO CODEC- ALC3281

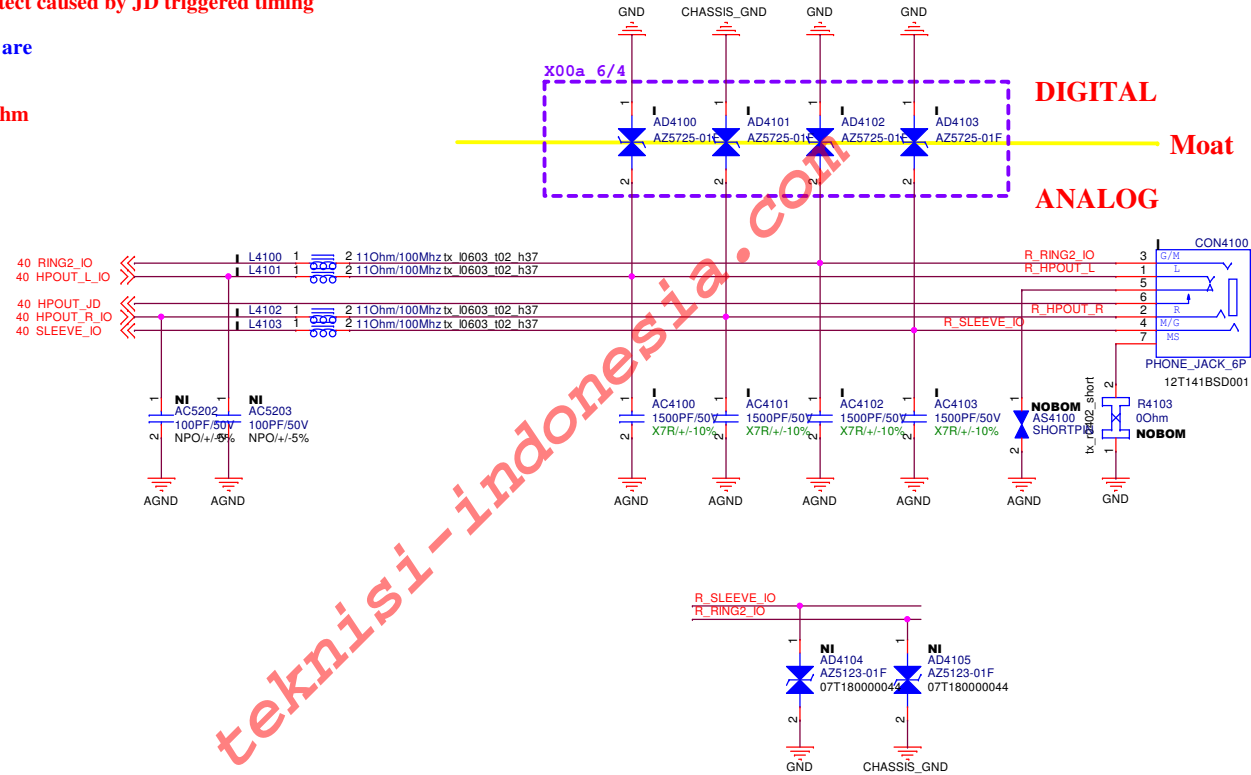


GLOBAL HEADSET CONNECTOR

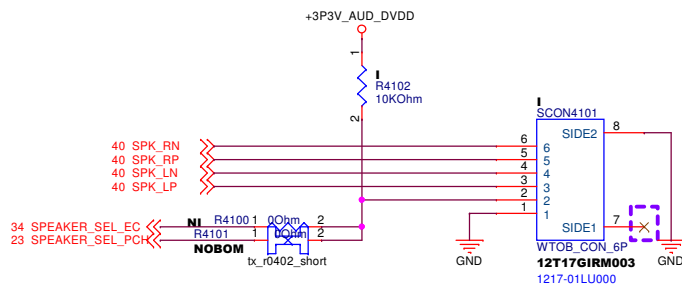
OMTP/CTIA headset, Headphone, Line-Out,
Microphone input, Line input.

This recommended phone-jack has moved #5/#6 Jack detect pin to the last position and lined up with #1 Tip pin.
This kind of design will significantly improve the false detect caused by JD triggered timing

PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are
required at least 40 mil for HP crosstalk consideration
and, its length should be as short as possible.
L4100/L4103 should choose DC resistance (R_{dc}) < 30m-ohm
to get the best audio performance for HP crosstalk.



SPEAKER CONN



	15" FG	15" Zylux	17" FG	17" VECO	BIOS/EE setting
1st source (Pin1 & 2 open)	V		V		Pull High
2nd source (Pin1 & 2 short)		V		V	Pull Low

<Core Design>

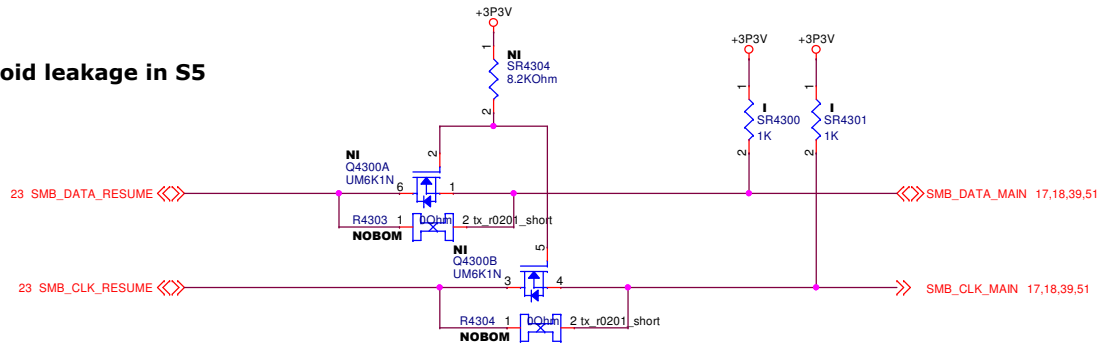
PEGATRON		Title : AUDIO JACK	
Pegatron Corp.		Engineer: Ryan_Yen	
Size A3	Project Name Orion_N18E	Rev A00	
Date: Friday, December 14, 2018		Sheet 41 of 93	

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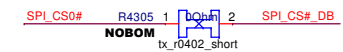
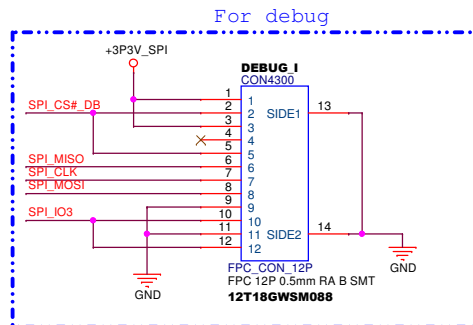
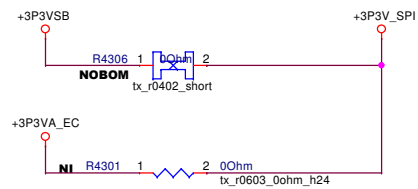
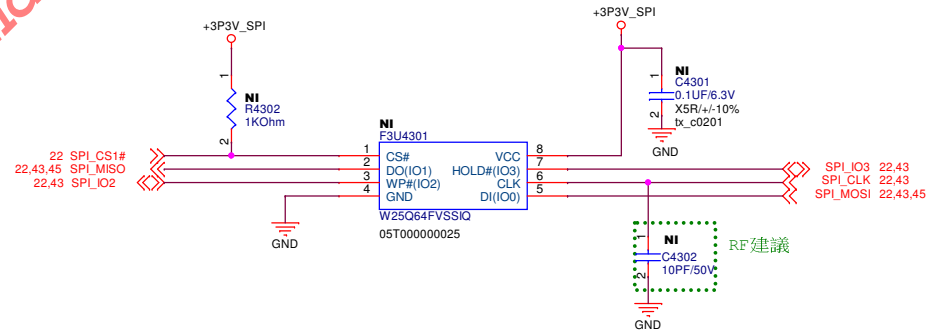
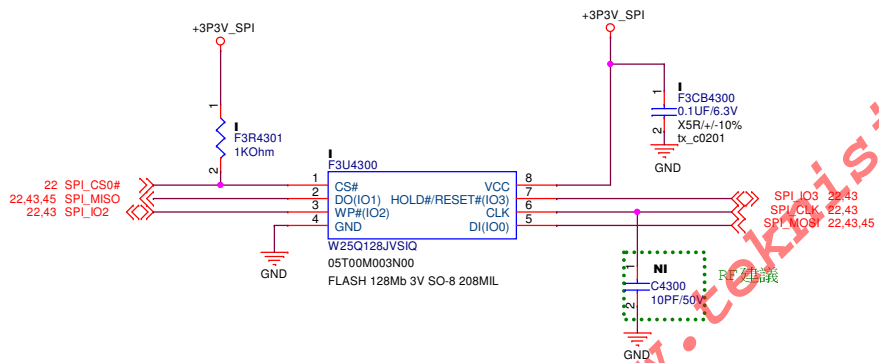
<Core Design>

PEGATRON		Title : USB Redriver	
Pegatron Corp.		Engineer: Ryan_Yen	
Size A3	Project Name Orion_N18E		Rev A00
Date: Friday, December 14, 2018		Sheet 42 of 93	

Avoid leakage in S5



SPI ROM (Quad I/O Supported)



PEGATRON DT-MB RESTRICTED SECRET

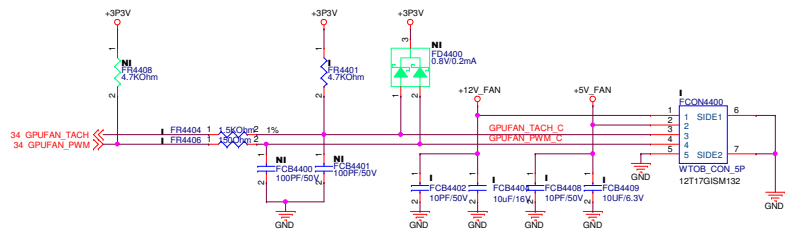
PEGATRON Title : SM BUS & SPI ROM

Pegatron Corp. **Engineer:** *Ryan_Yen*

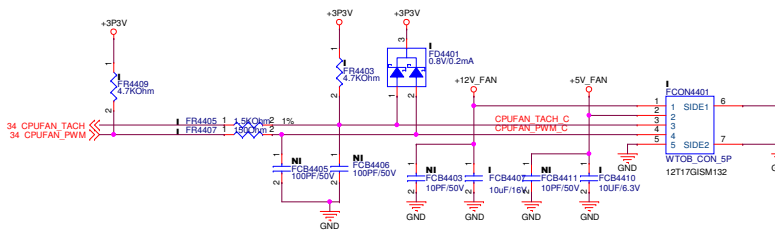
Size A3	Project Name Orion_N18E	Rev A00
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Date: Friday, December 14, 2018 Sheet 43 of 93

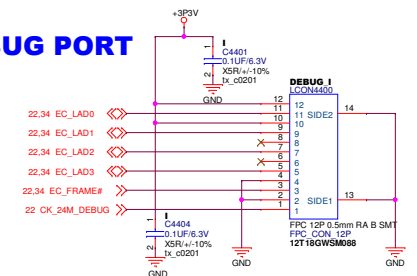
GPU FAN CONNECTOR



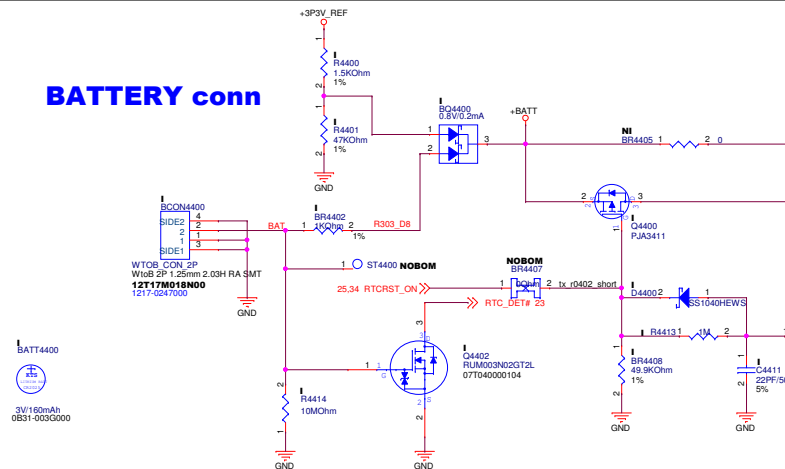
CPU FAN CONNECTOR



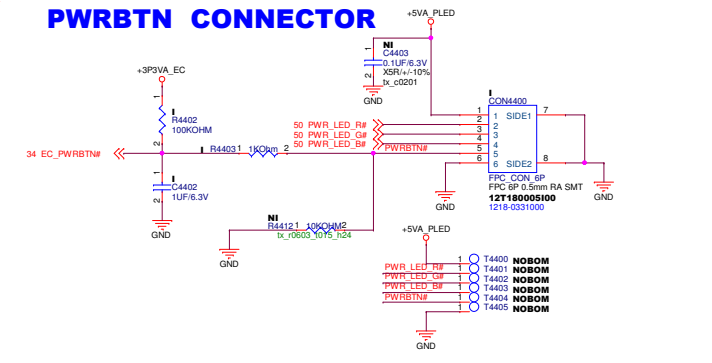
LPC DEBUG PORT



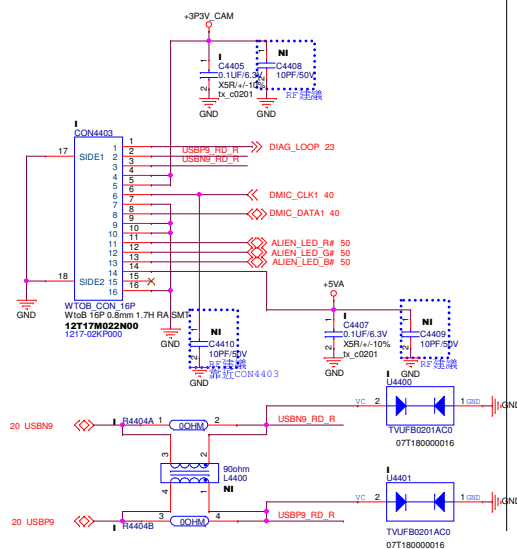
BATTERY conn



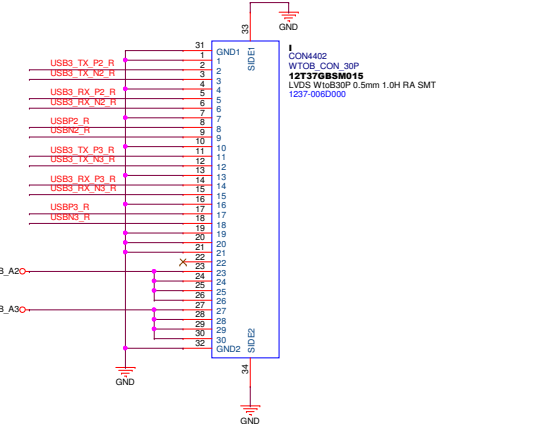
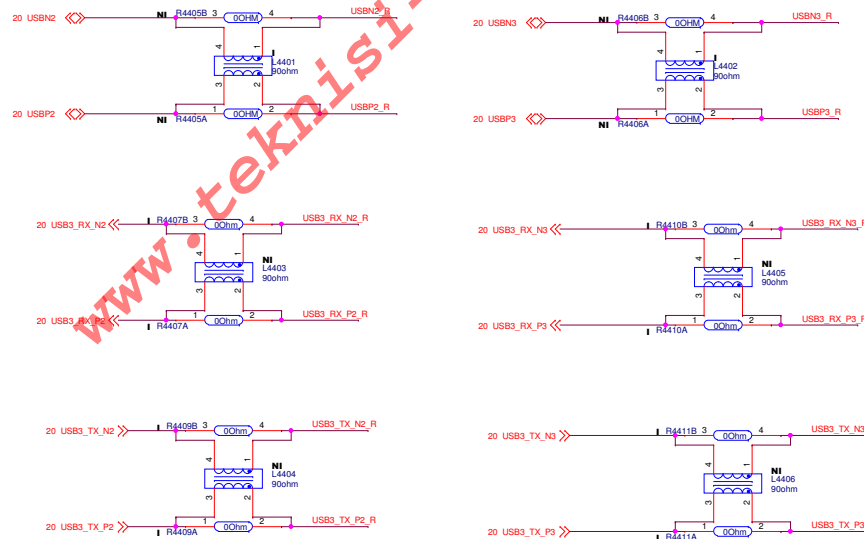
PWRBTN CONNECTOR



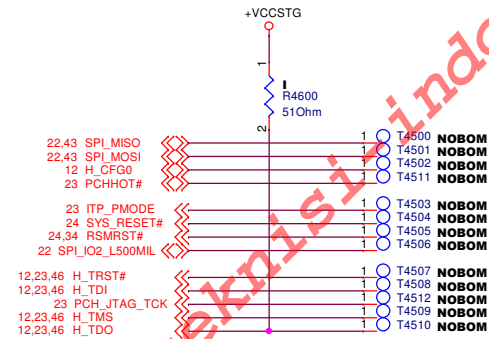
CAMERA & DMIC CONNECTOR



CARD - USB CON



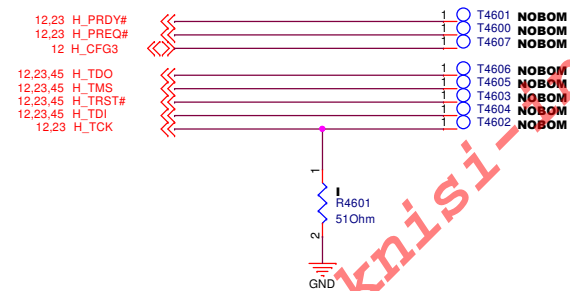
INTEL PCH DEBUG TESTPOINT



<Core Design>

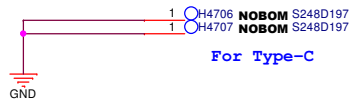
PEGATRON		Title : DEBUG TESTPOINT(PCH)	
Pegatron Corp.		Engineer: Ryan_Yen	
Size A3	Project Name Orion_N18E	Rev A00	
Date: Friday, December 14, 2018	Sheet 45 of 93		

INTEL CPU DEBUG TESTPOINT

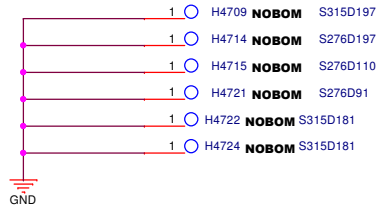


NI_TEMP
PCB4700
PCB
PCB_BOARD
CCL = Y

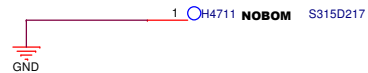
方圓孔 (6.3*6.3, D2.3) 靠近CON3000 (USB TYPE-C) · 2顆



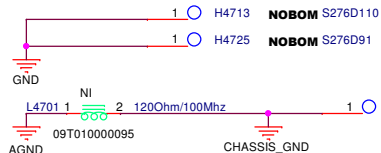
方圓孔 (7*7, D2.3), 1顆
方圓孔 (8*8, D5), 1顆
方圓孔 (7*7, D5), 1顆
方圓孔 (7*7, D2.8), 1顆
方圓孔 (8.8, D4.2), 2顆



方圓孔 (8*8, D5.5), 1顆



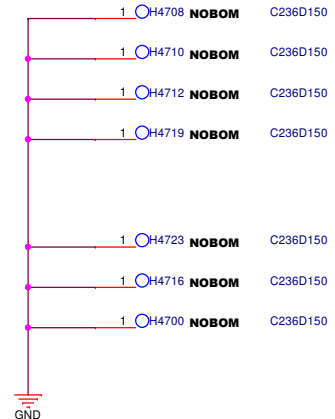
方圓孔 (7*7, D2.8), 4顆



圓孔 2.0mm · 1顆



圓孔 (6*6, D3.8), 7顆

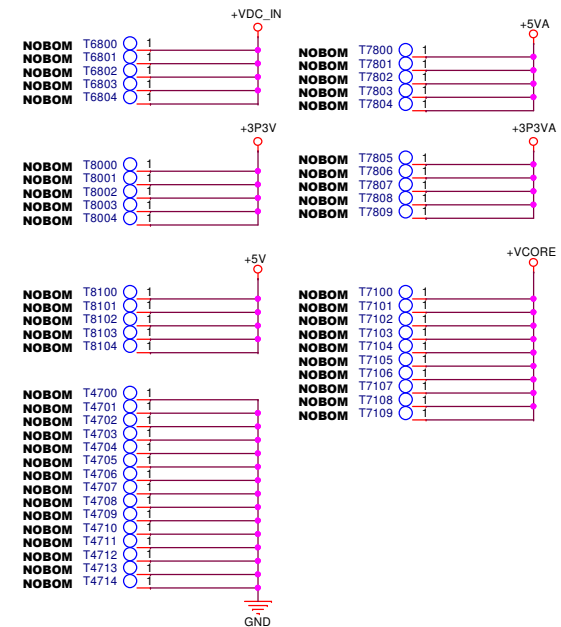
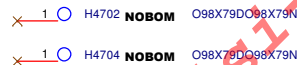


For CPU

For GPU

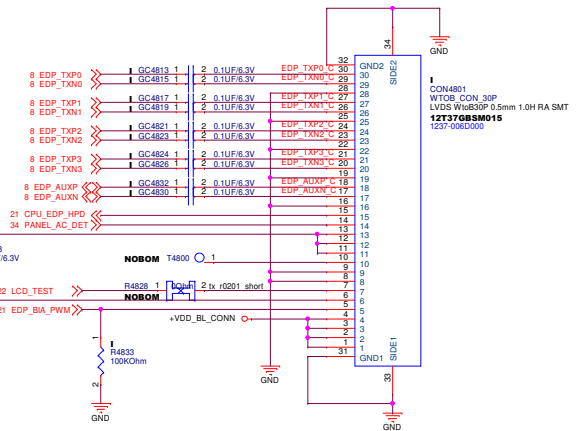
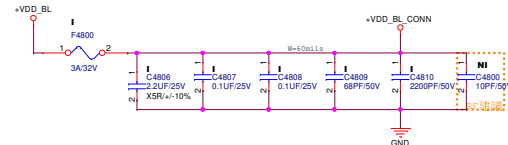
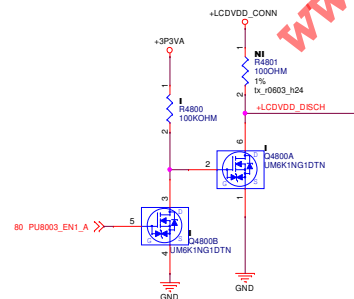
PPID

橢圓孔 2.5mm*2.0mm · 2顆

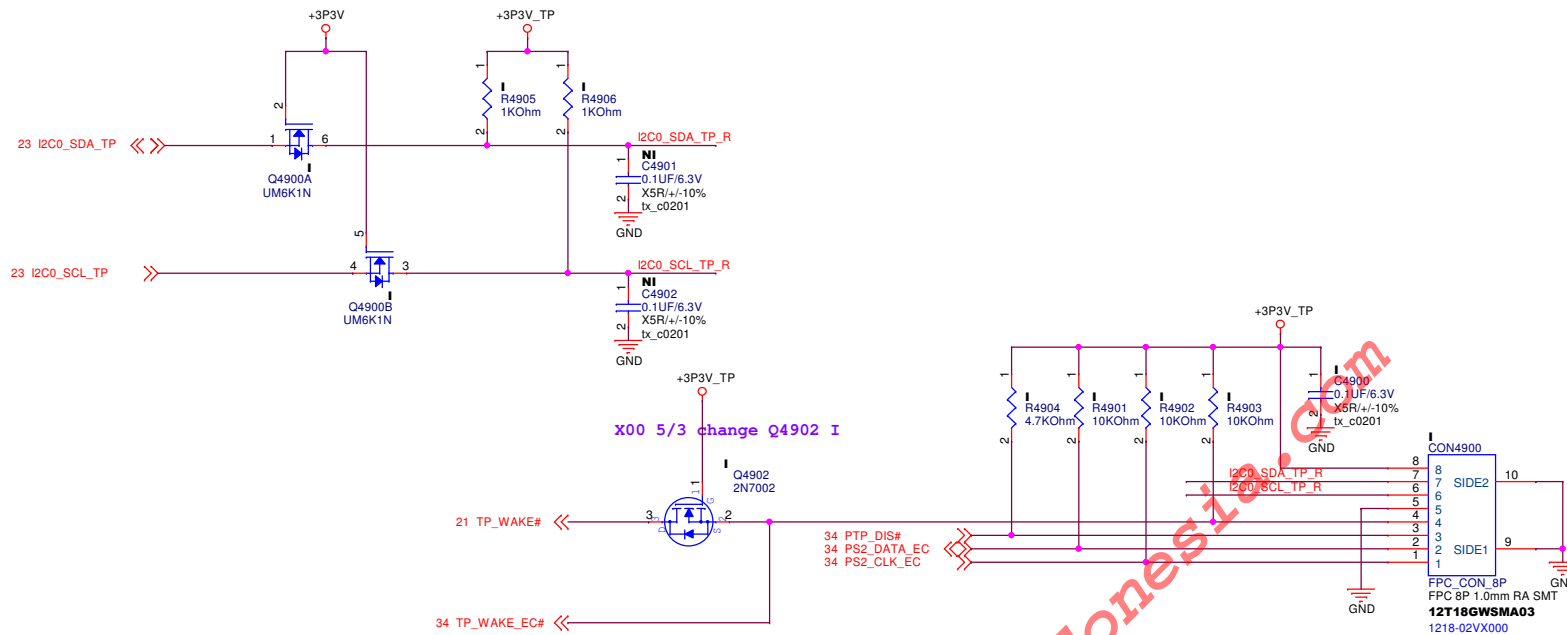


PEGATRON DT-MB RESTRICTED SECRET

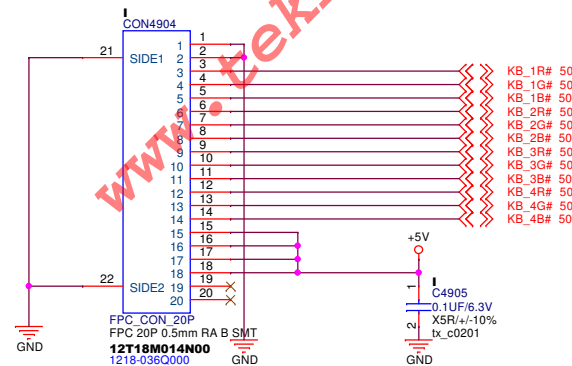
PEGATRON		Title : PCB & Label & Screw	
Pegatron Corp.		Engineer: Ryan_Yen	
Size A3	Project Name Orion_N18E	Date: Friday, December 14, 2018	Rev A00
Sheet 47 of 93			



Pegatron Corp.		Project Name		Rev
Size		Project Name		Rev
A2		Orion_N18E		A00
Date: Friday, December 14, 2018		Sheet		48 of 93

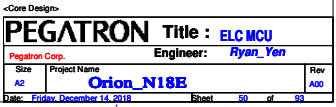


Touch Pad



Keyboard backlight

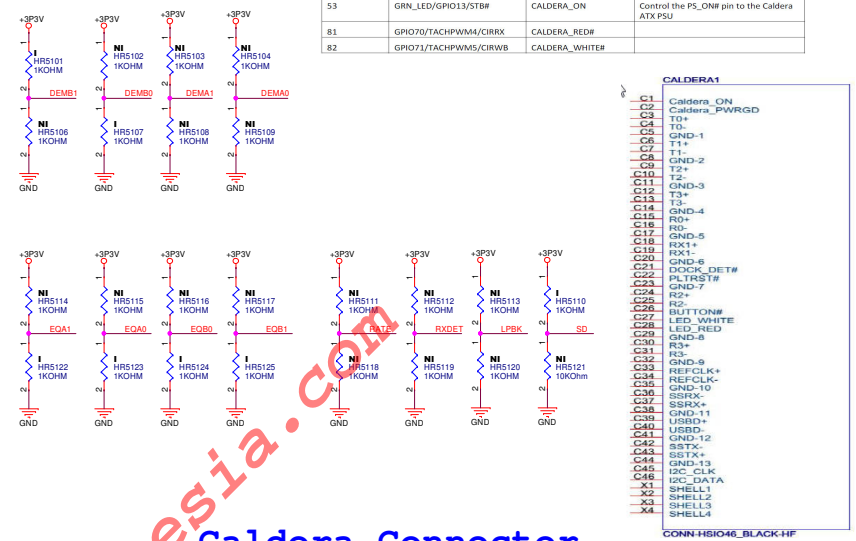
<Core Design>			
PEGATRON		Title : Touch & Keyboard BL	
Pegatron Corp.		Engineer: Ryan_Yen	
Size A3	Project Name Orion_N18E		Rev A00
Date: Friday, December 14, 2018		Sheet	49 of 93



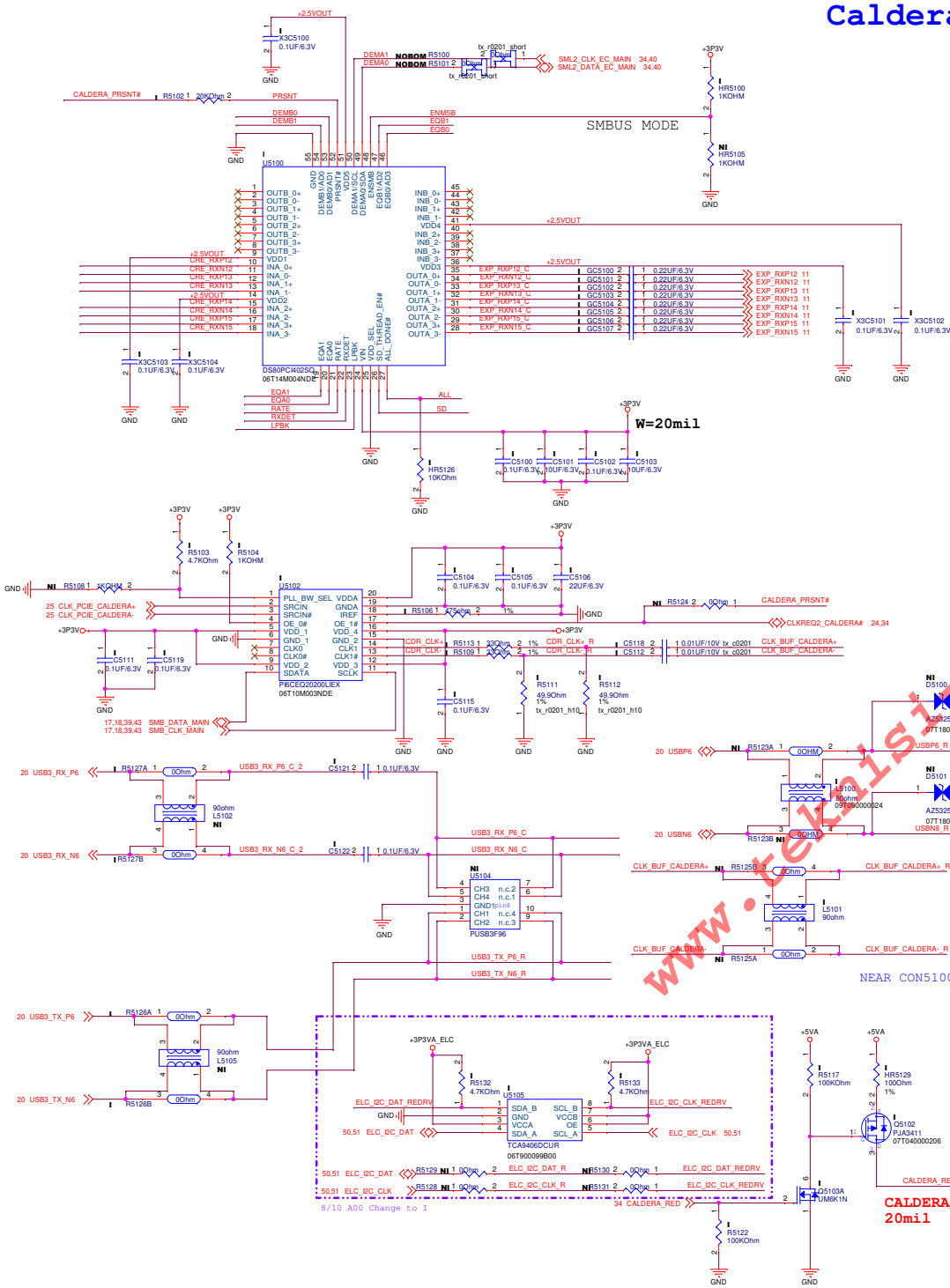
Caldera Redriver

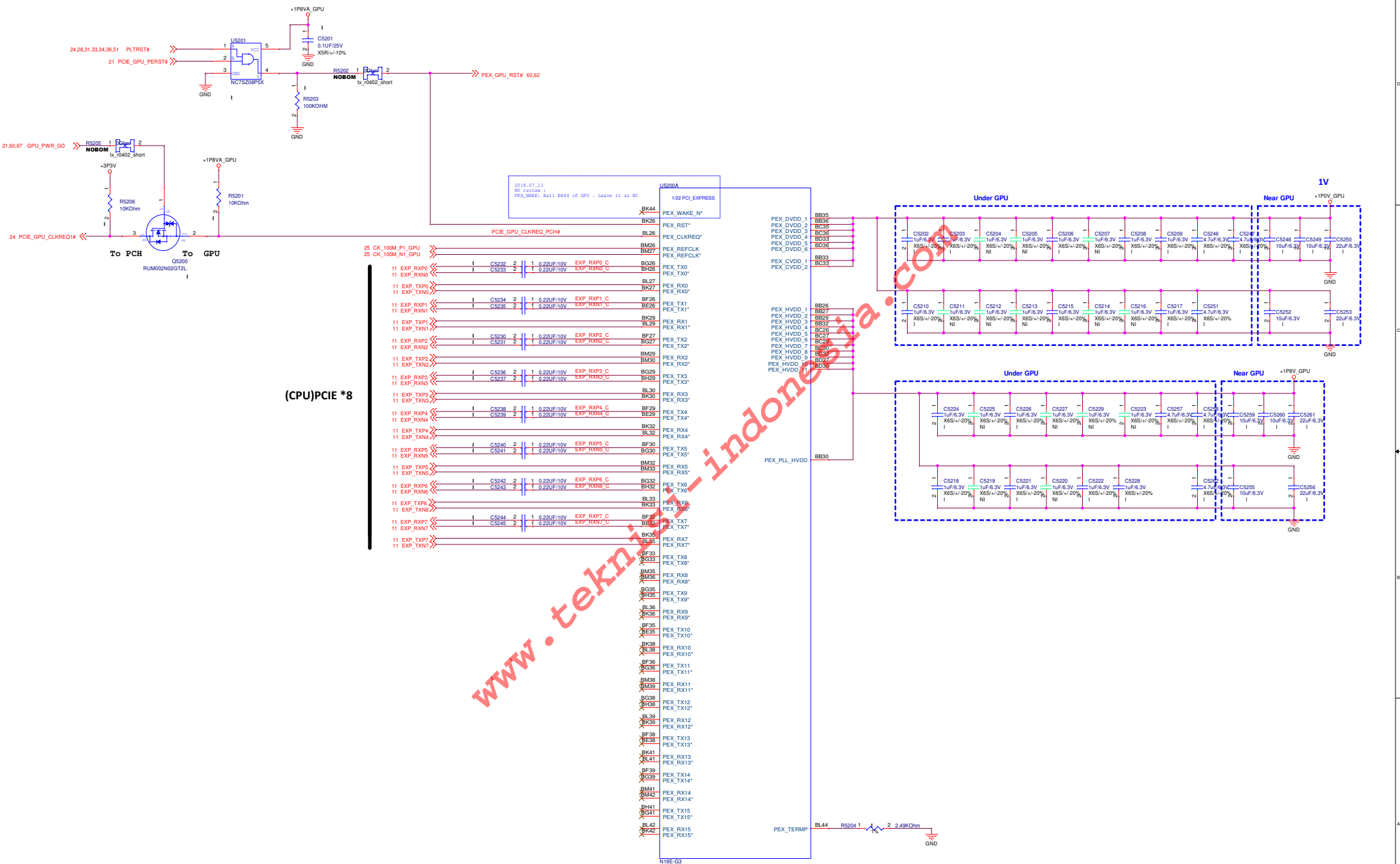
Pin Number	SIO Definition	Usage for Caldera	Comment
37	YLW_LED/GPIO30/S1CT	CALDERA_BUTTON#	User will press this button when they want to initiate an undock event
38	GPIO31/PE/P2_D0L#	CALDERA_PSRNT#	Use for internal cable-detect mechanism
39	GPIO32/BU5Y/P2_D0L#	CALDERA_PWRGD	
53	GRN_LED/GPIO13/STB#	CALDERA_ON	Control the PS_ON# pin to the Caldera ATX PSU
81	GPIO70/TACHPWM4/CIRRX	CALDERA_RED#	
82	GPIO73/TACHPWM5/CIRWB	CALDERA_WHITE#	

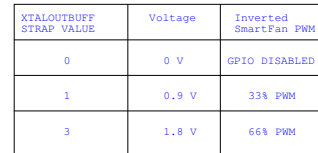
Pin #	Name
C46	I2C_CLK
C45	I2C_CLK
C44	GND
C43	SSRX-
C42	SSRX+
C41	GND
C40	USB D+
C39	USB D-
C38	GND
C37	SSTX-
C36	SSTX+
C35	GND
C34	REFCLK-
C33	REFCLK+
C32	GND
C31	R3-
C30	R3+
C29	GND
C28	LED RED
C27	LED WHITE
C26	BUTTON#
C25	R2-
C24	R2+
C23	GND
C22	PLTRST#
C21	DOCK_DET#
C20	GND
C19	R1-
C18	R1+
C17	GND
C16	R0-
C15	R0+
C14	GND
C13	T3-
C12	T3+
C11	GND
C10	T2-
C9	T2+
C8	GND
C7	T1-
C6	T1+
C5	GND
C4	T0-
C3	T0+
C2	Caldera_PWRGD
C1	Caldera_ON



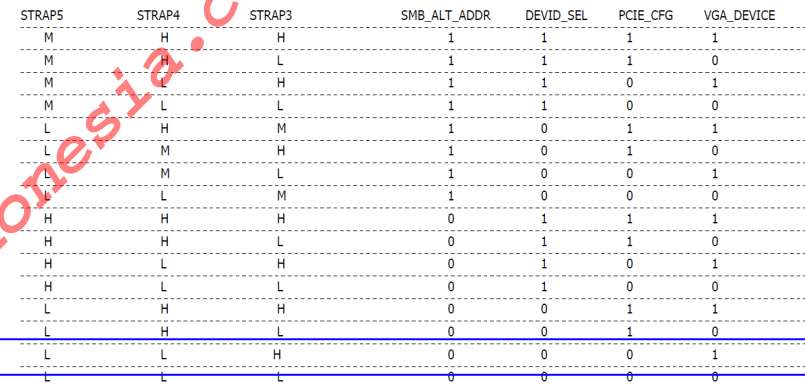
Caldera Connector







Strap Pins <small>see Note</small>			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)

[illegible]

```
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

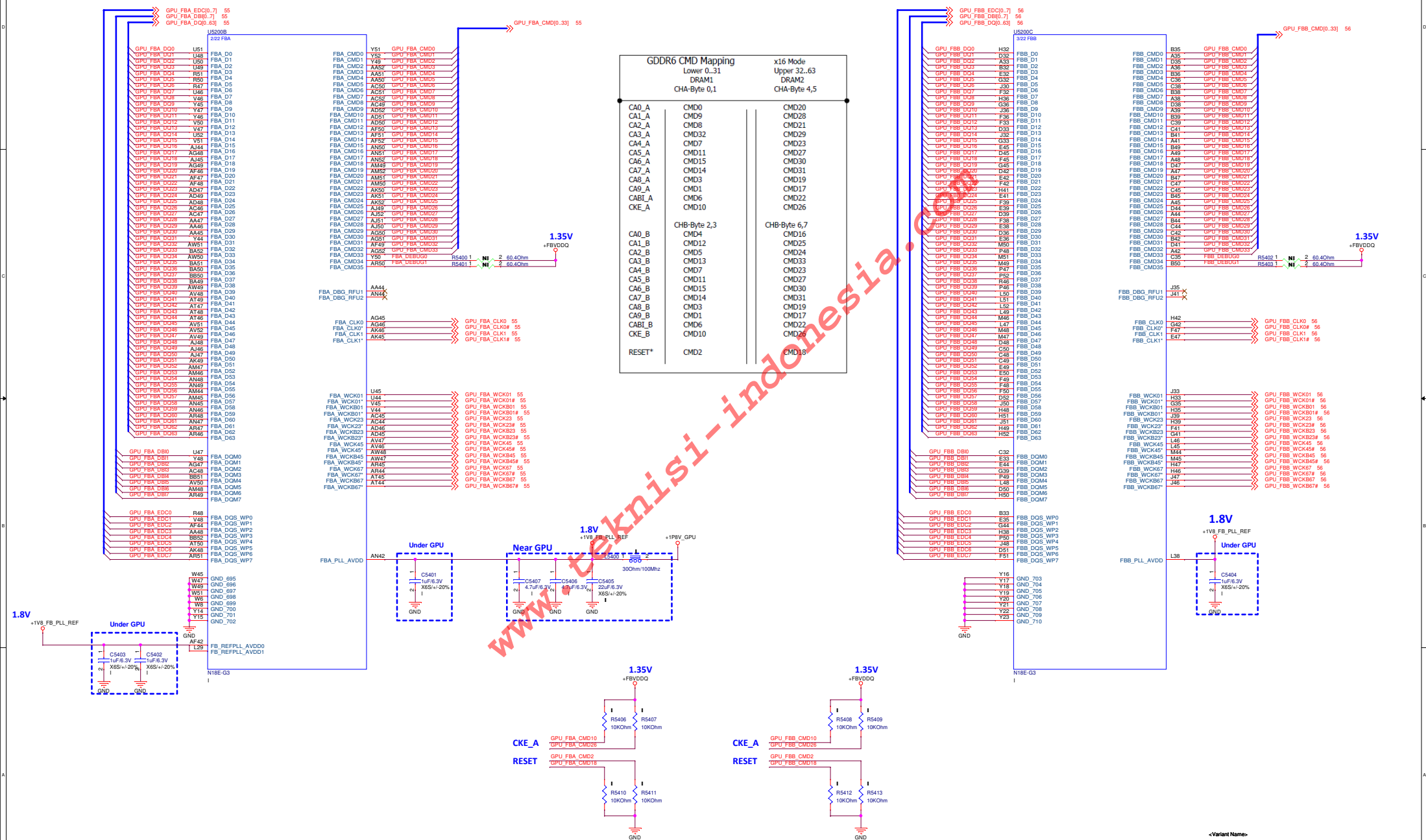
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

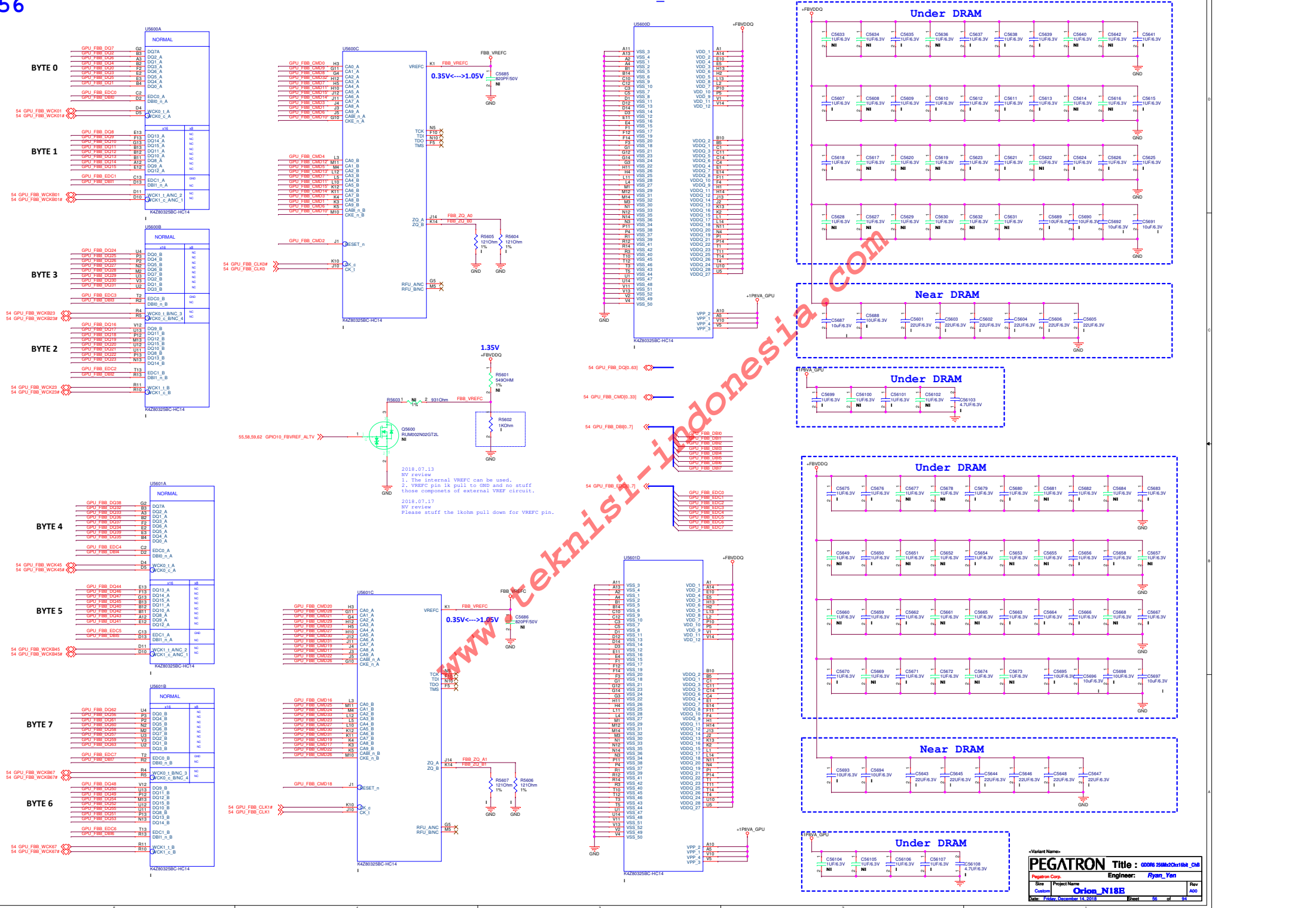
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

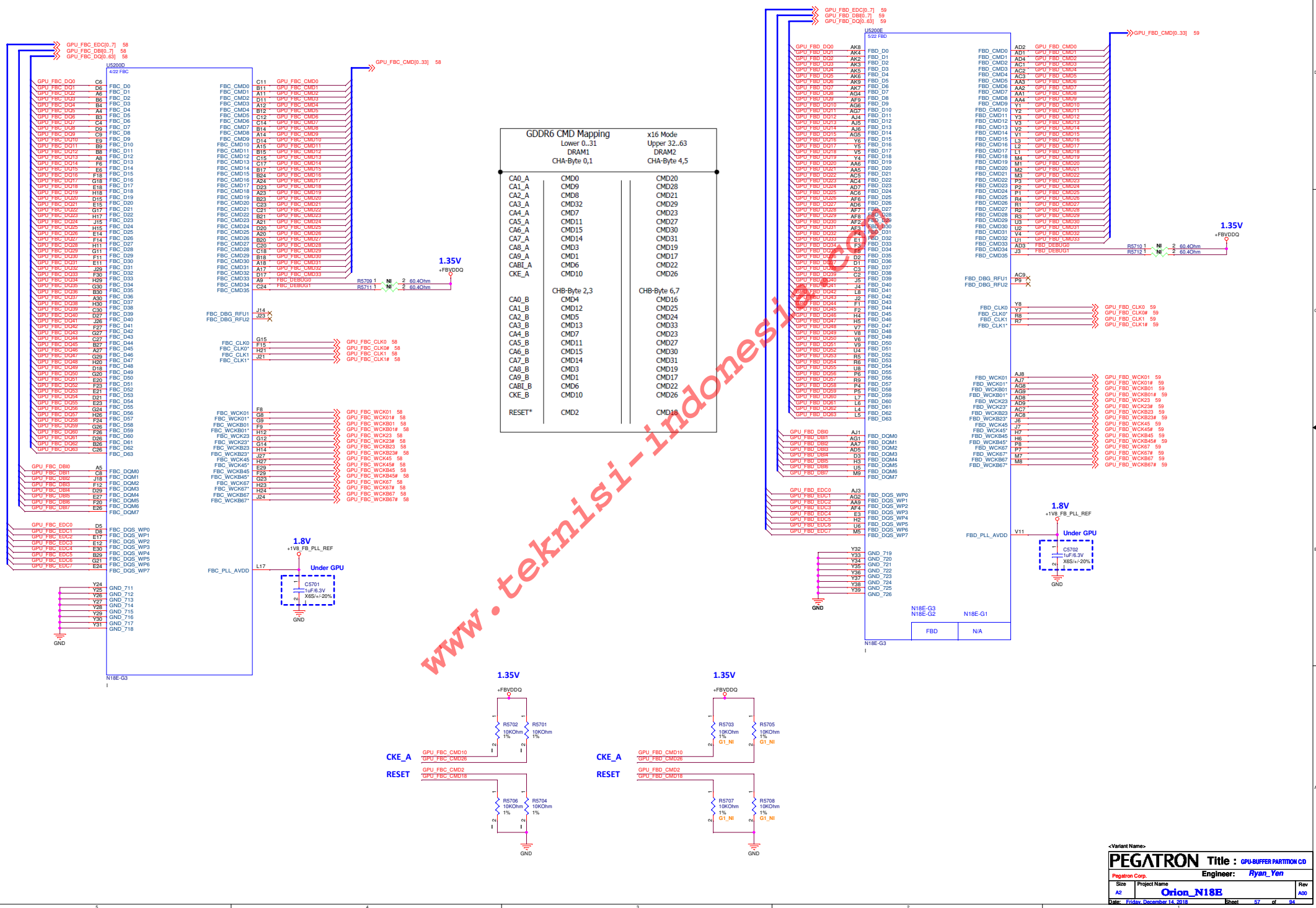
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
```

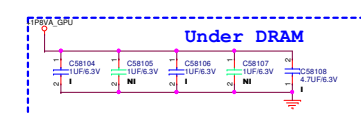
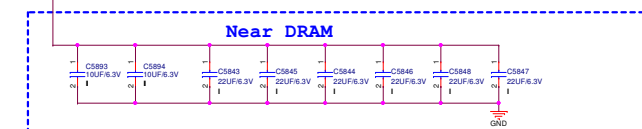
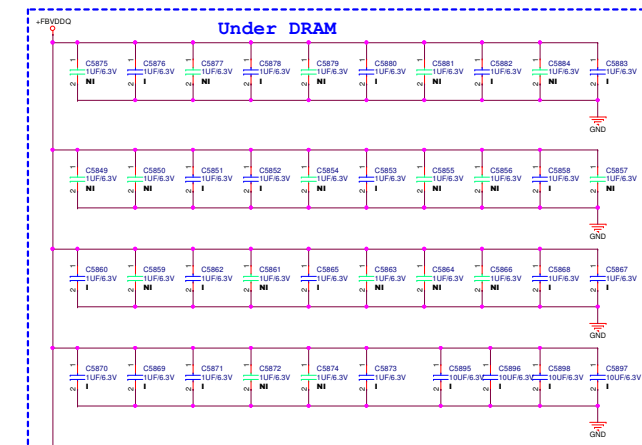
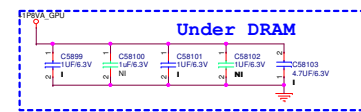
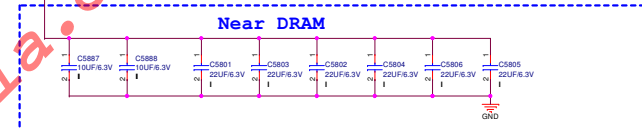
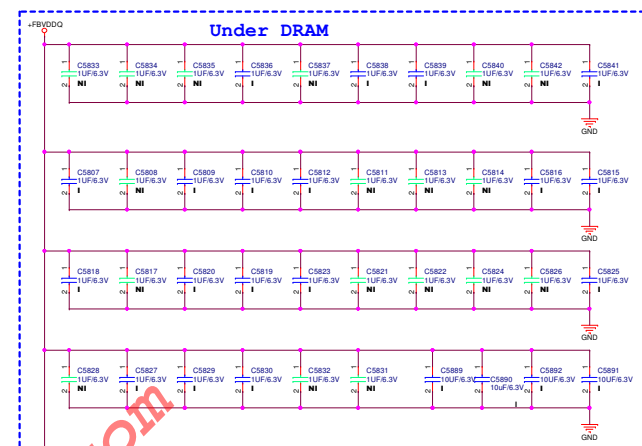
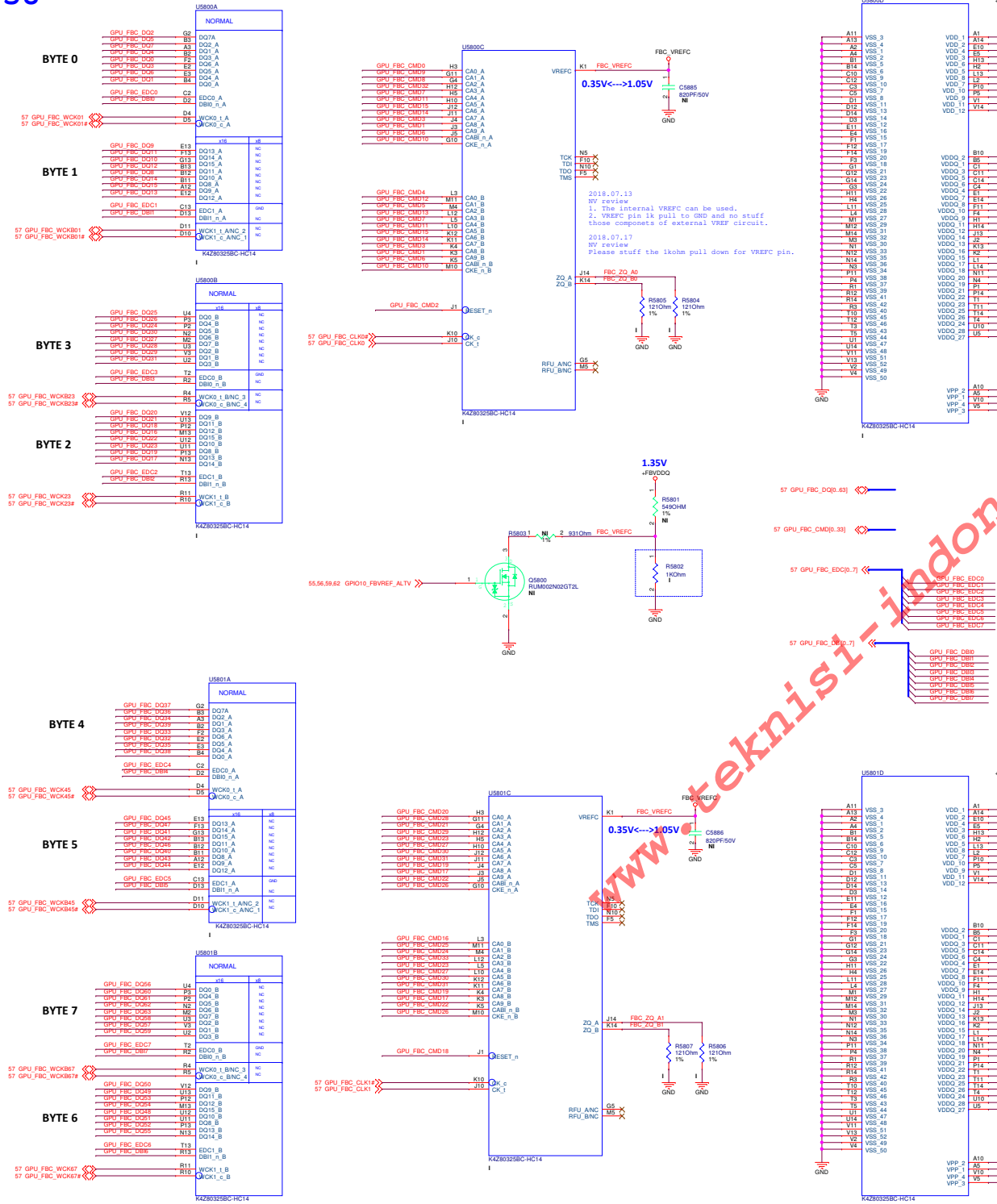
Memory Density	Allowed Memory Configuration	FBDVD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx2Chx16	1.35V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

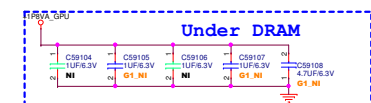
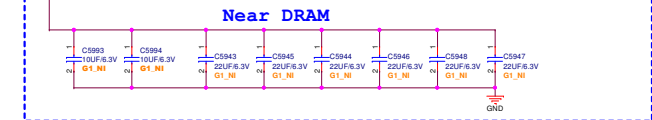
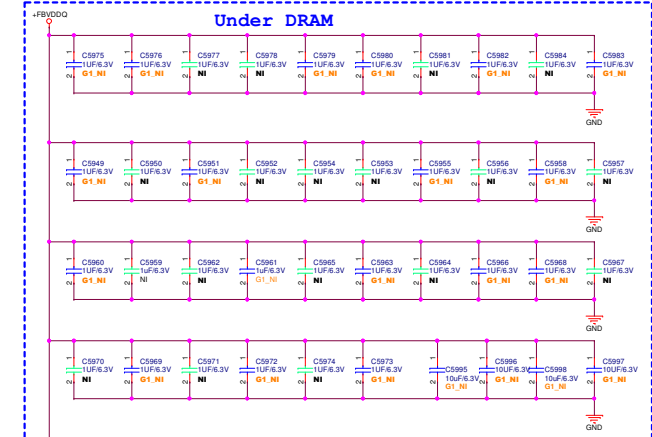
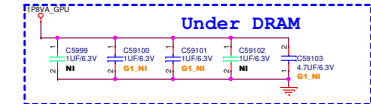
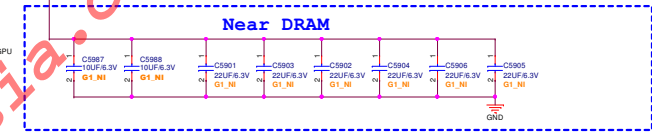
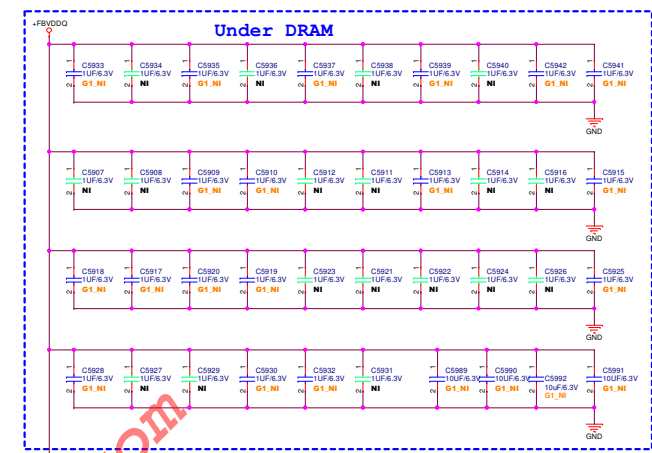
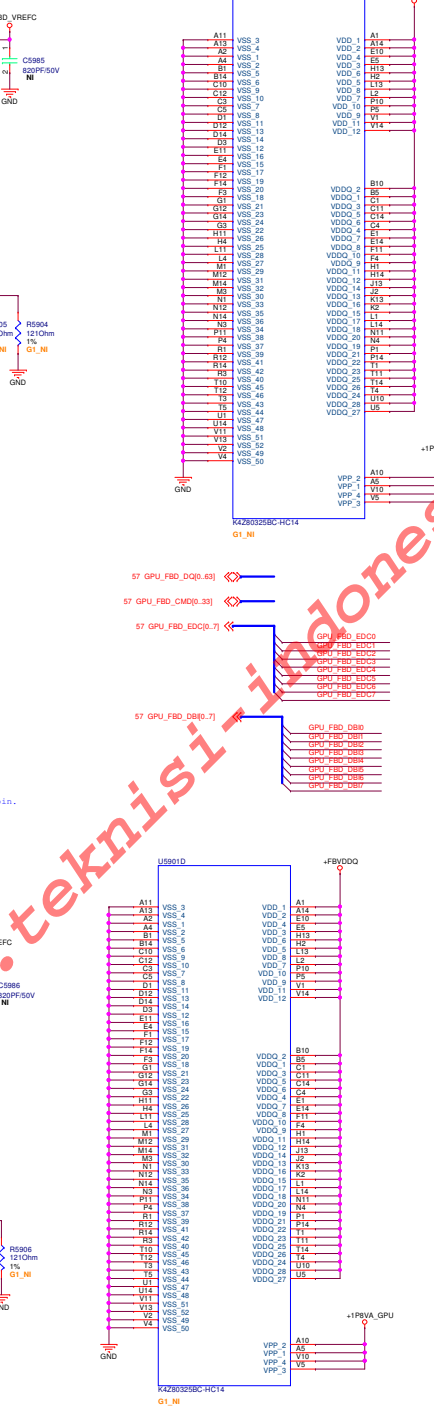
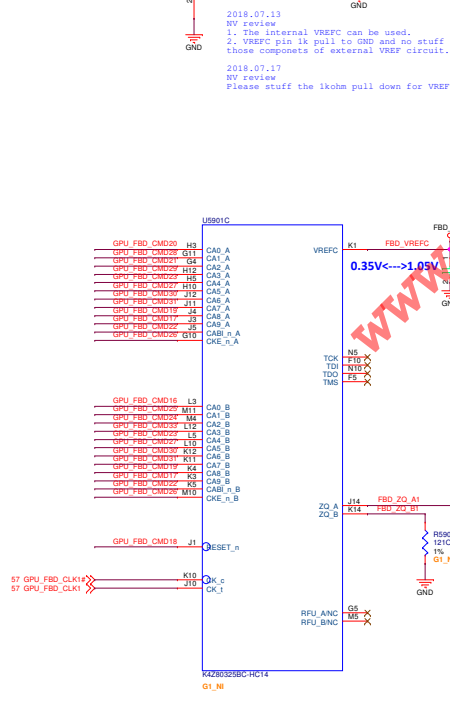
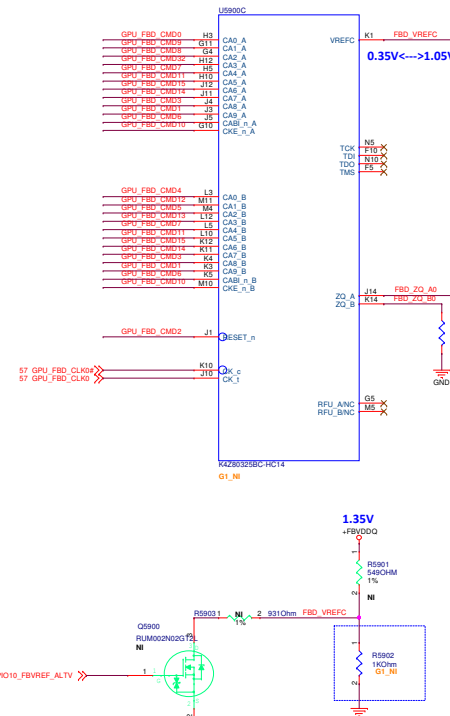
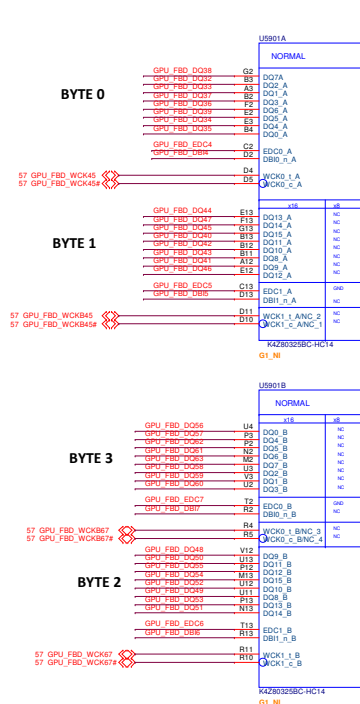
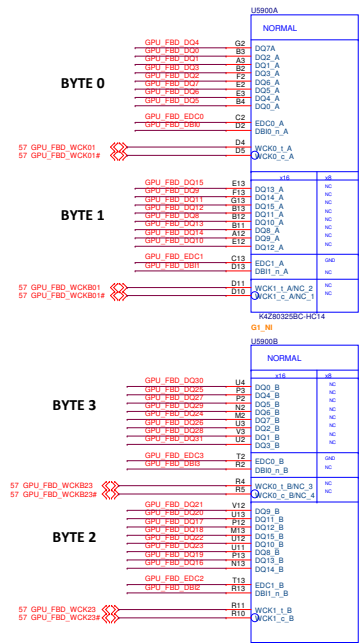
1. For N18E-G3, the maximum allowable memory case temperature is 95 °C.





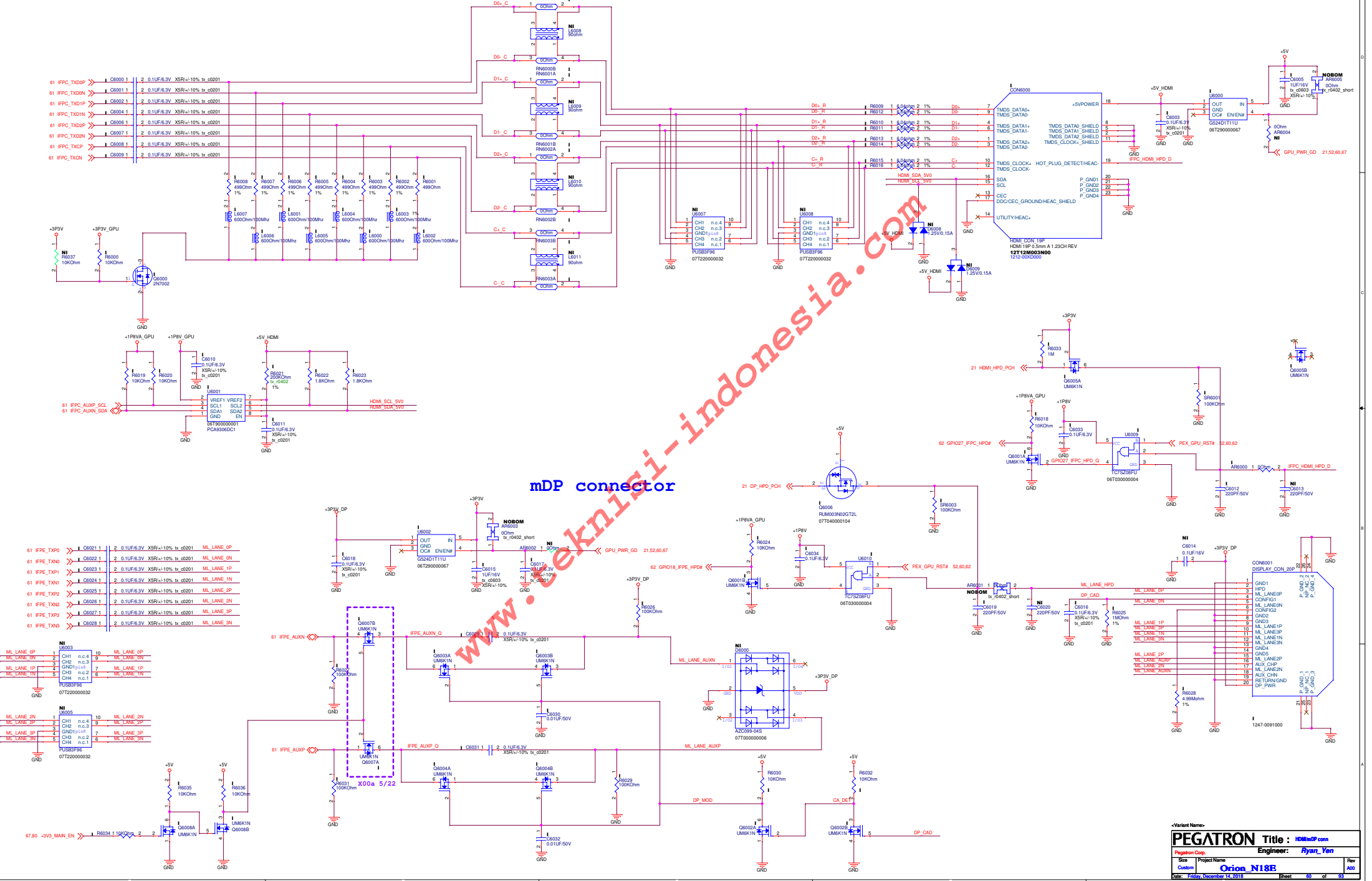


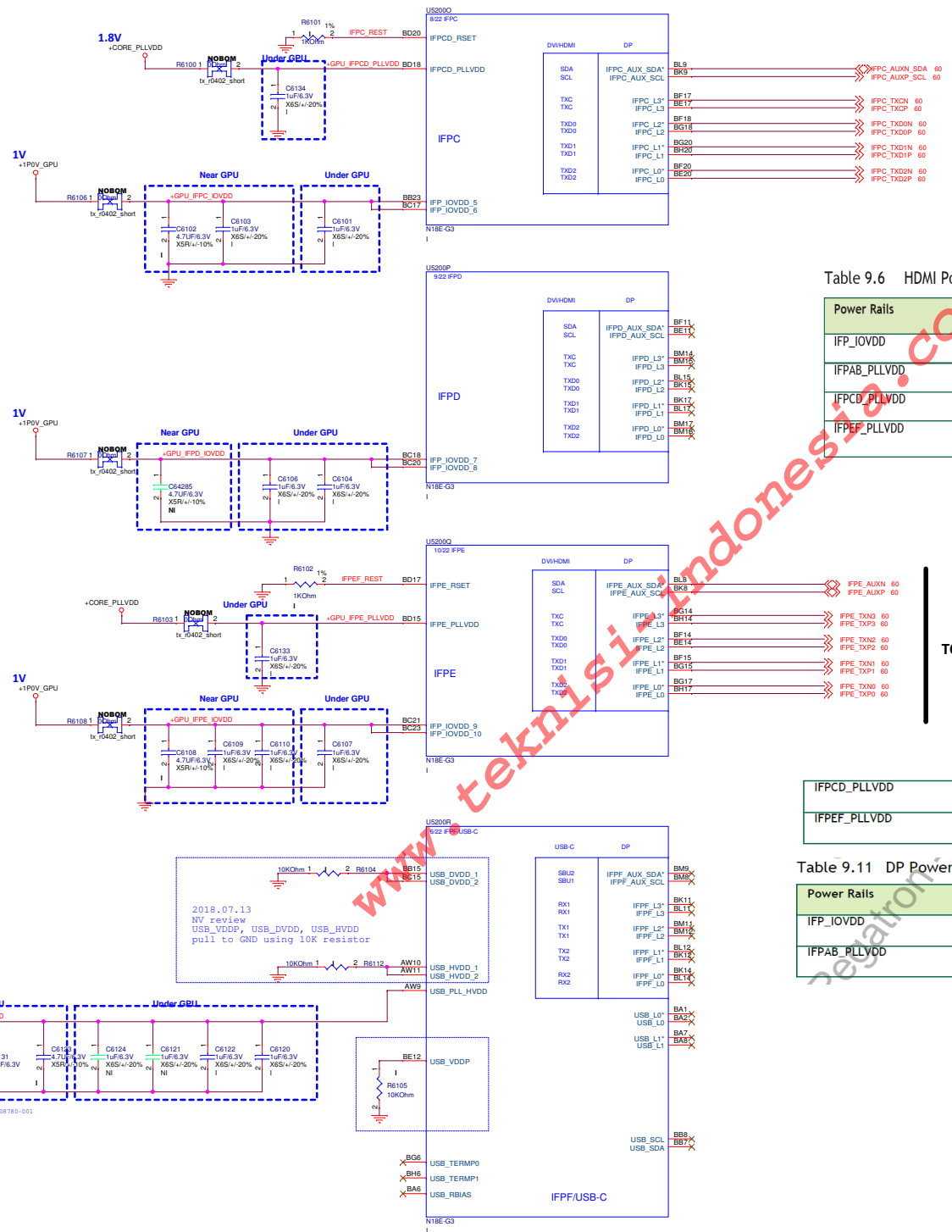




HDMI/MDP conn

HDMI out connector





TO HDMI

TO mDP

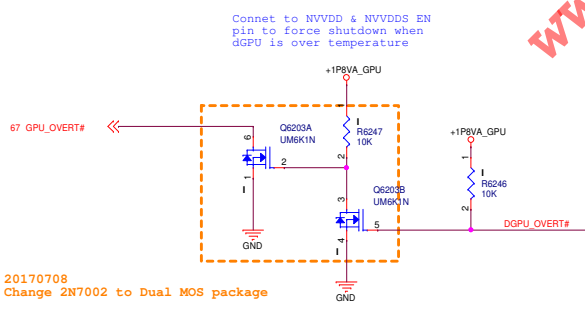
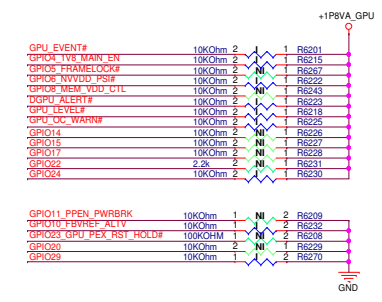
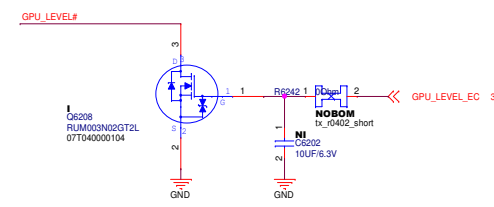
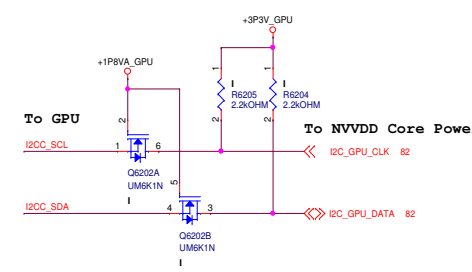
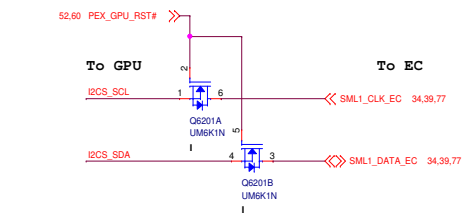
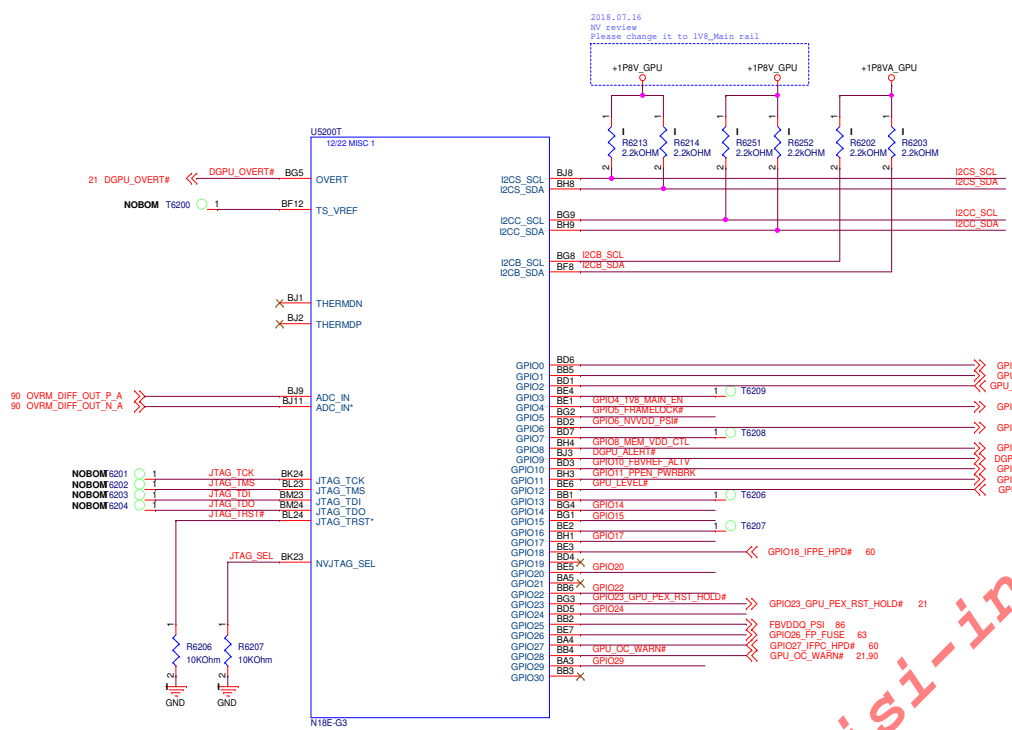
Table 9.6 HDMI Power Rails

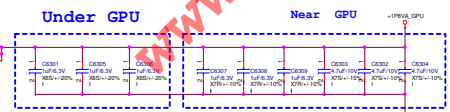
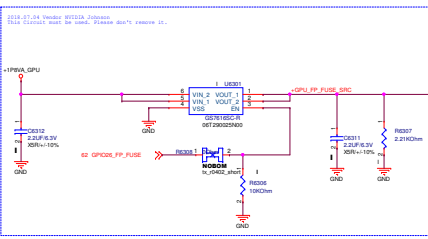
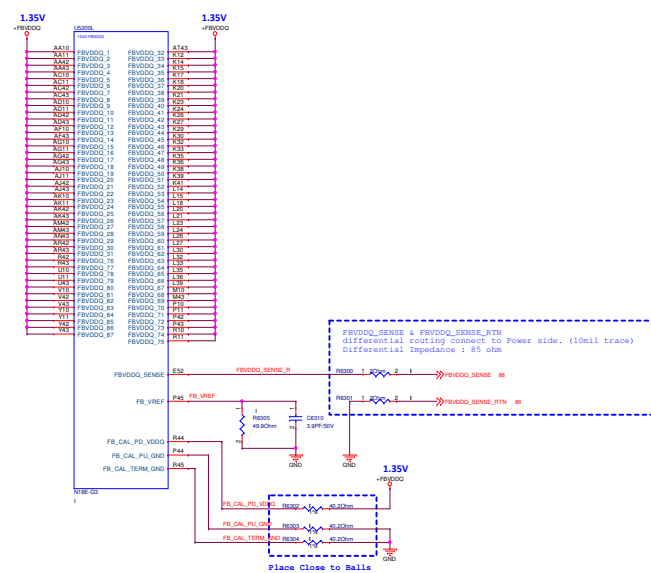
Power Rails	Voltage	Maximum Current Draw
IFPD_IOVDD	1.0 V ± 5%	~87 mA
IFPAB_PLLVDD	1.8 V ± 10%	~98 mA
IFPCD_PLLVDD	1.8 V ± 10%	~98 mA
IFPEF_PLLVDD	1.8 V ± 10%	~98 mA

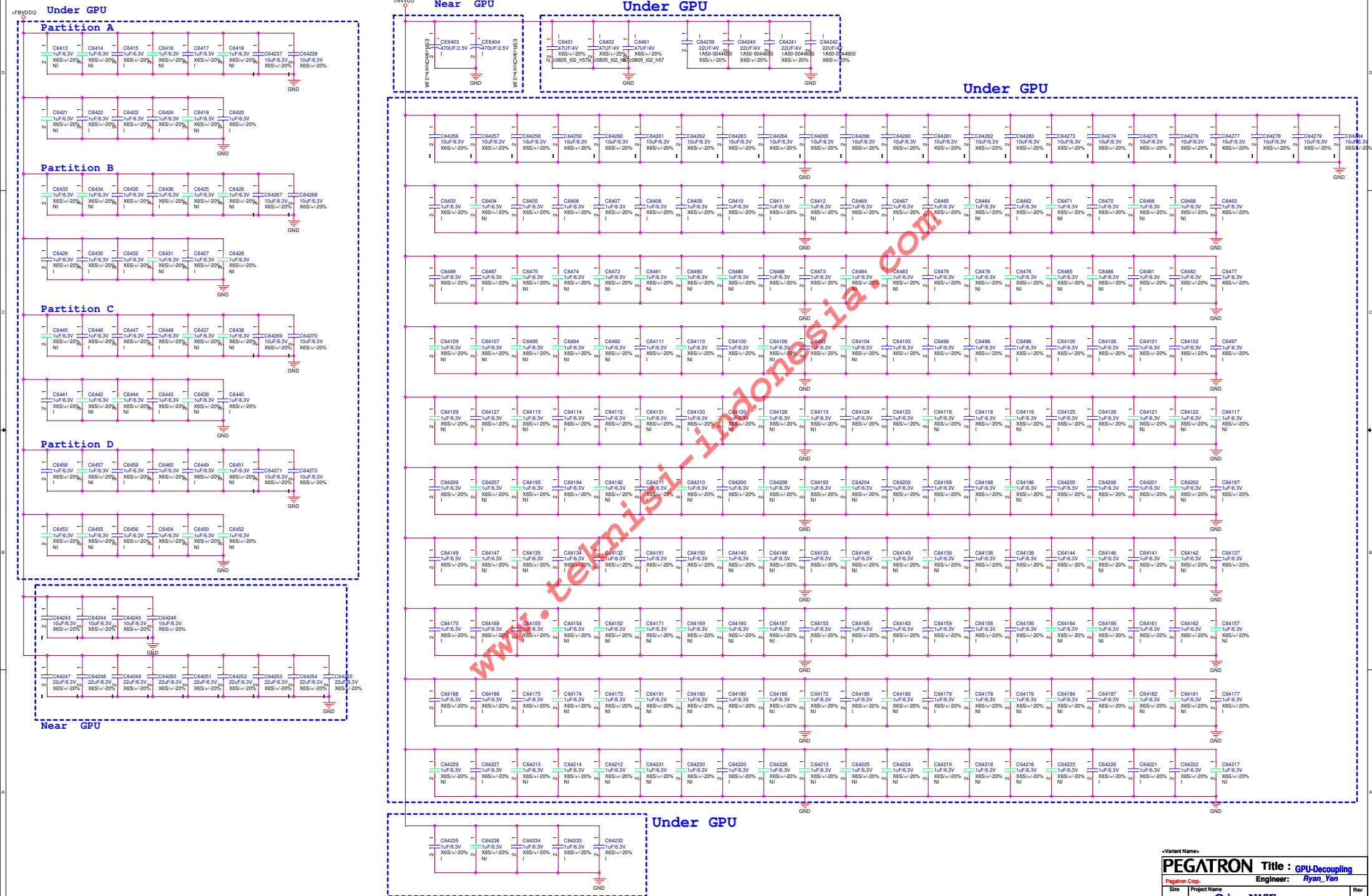
IFPCD_PLLVDD	1V8 V ± 10%	~102 mA
IFPEF_PLLVDD	1V8 V ± 10%	~102 mA

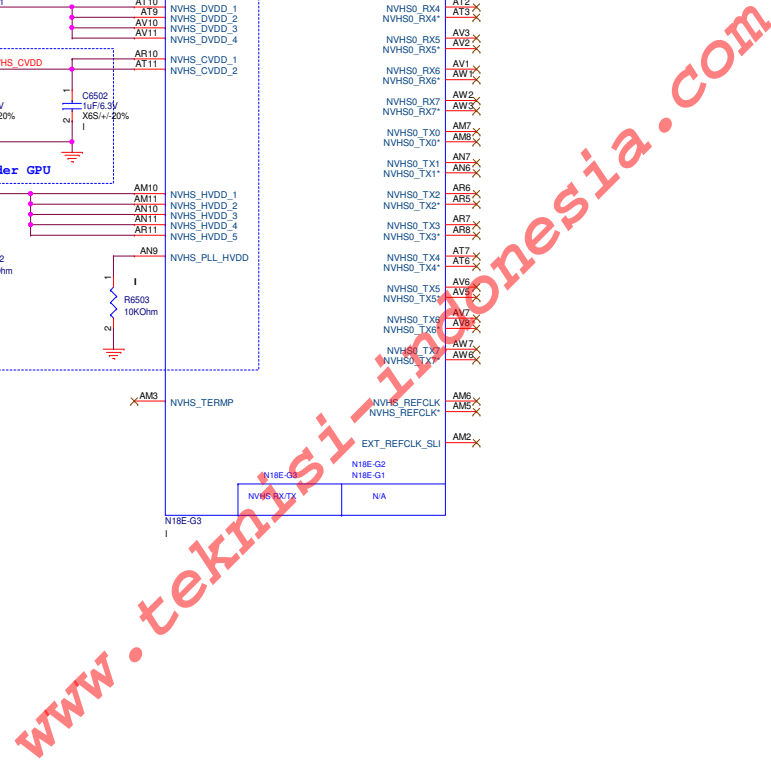
Table 9.11 DP Power Rails

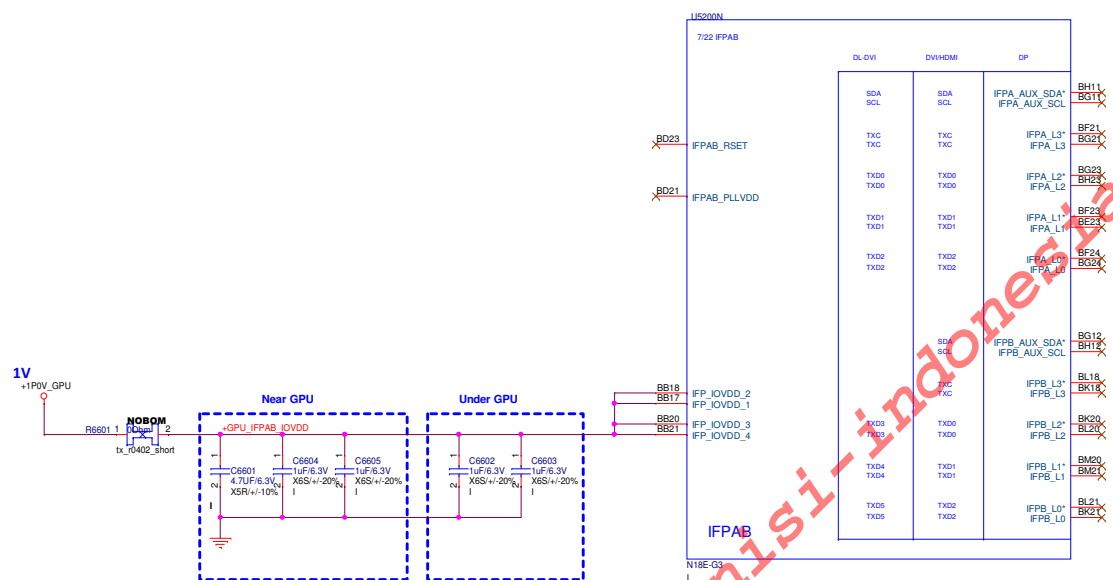
Power Rails	Voltage	Maximum Current Draw
IFPD_IOVDD	1.0 V ± 5%	~118 mA
IFPAB_PLLVDD	1V8 V ± 10%	~102 mA





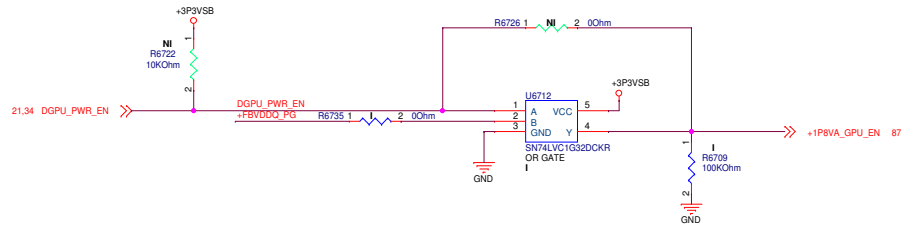




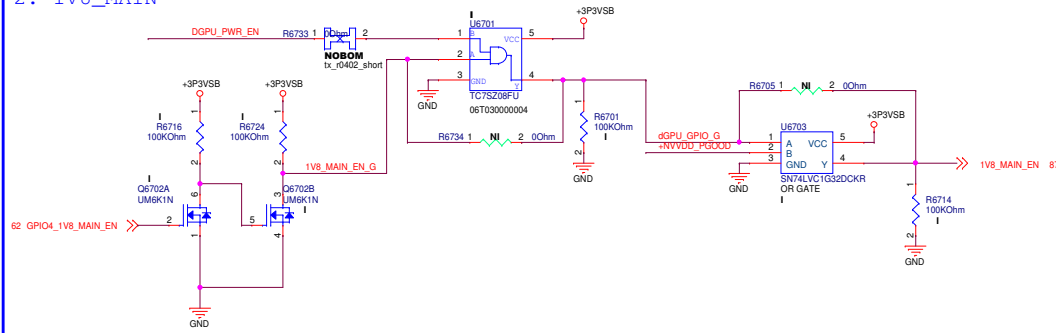


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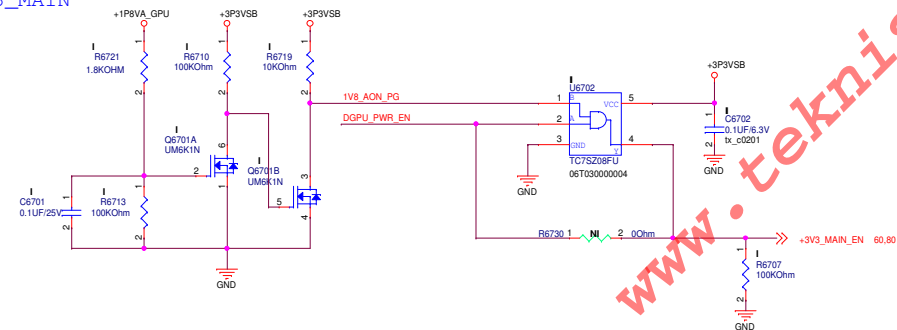
1. 1V8_AON



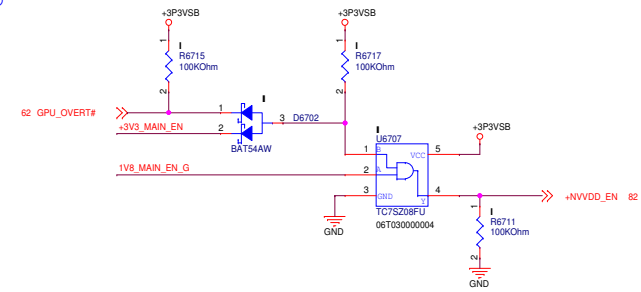
2. 1V8_MAIN



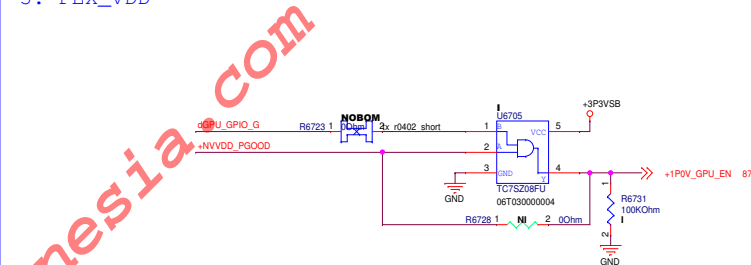
3. 3V3_MAIN



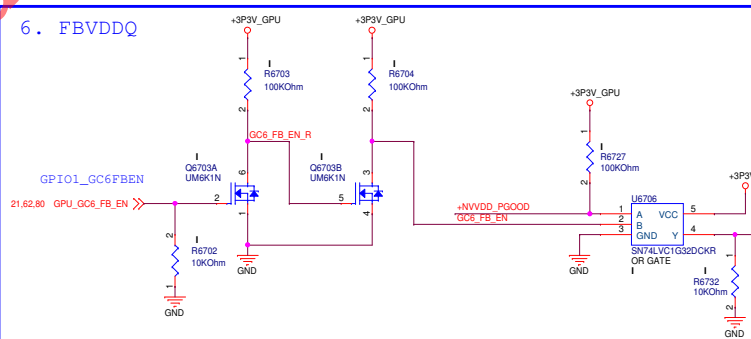
4. NVVDD



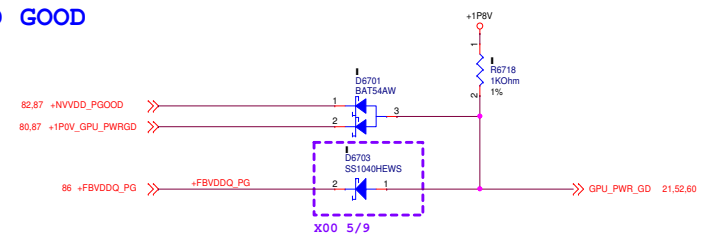
5. PEX_VDD



6. FBVDDQ



BOARD GOOD



<Variant Name>

PEGATRON Title : GPU_POWER Sequence

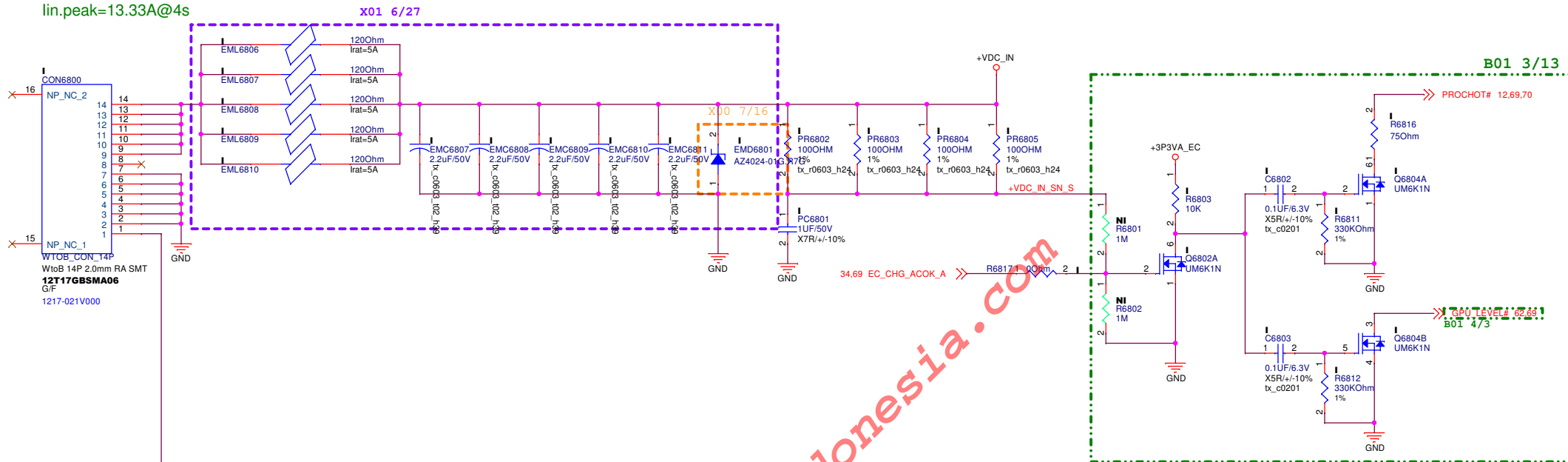
Pegatron Corp. Engineer: Ryan_Yen

Size Project Name Orion_N18E Rev A00

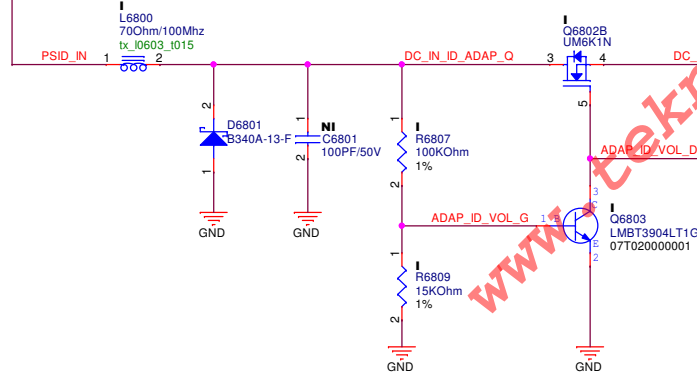
Date: Friday, December 14, 2018 Sheet 67 of 94

DC-IN connector

lin.cont= 12.31A
lin.peak=13.33A@4s

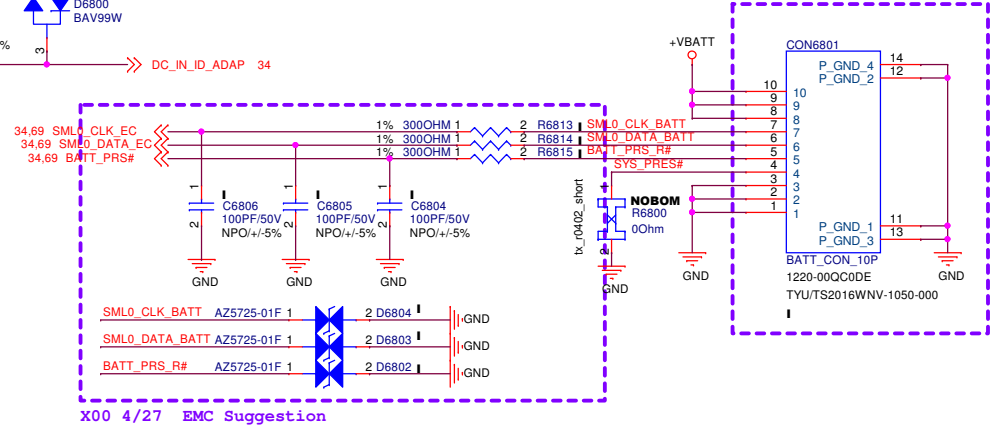


PSID Circuit

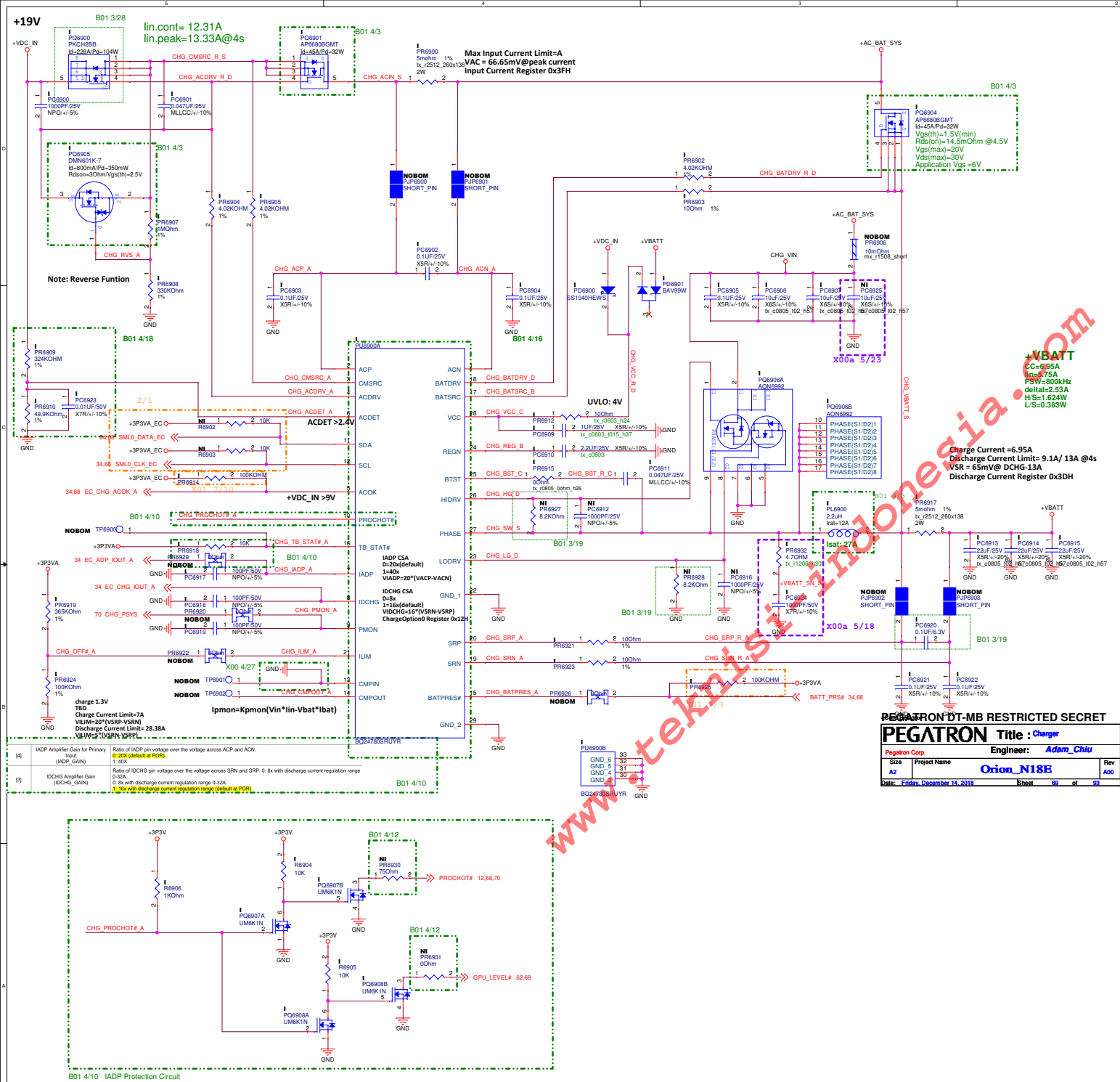


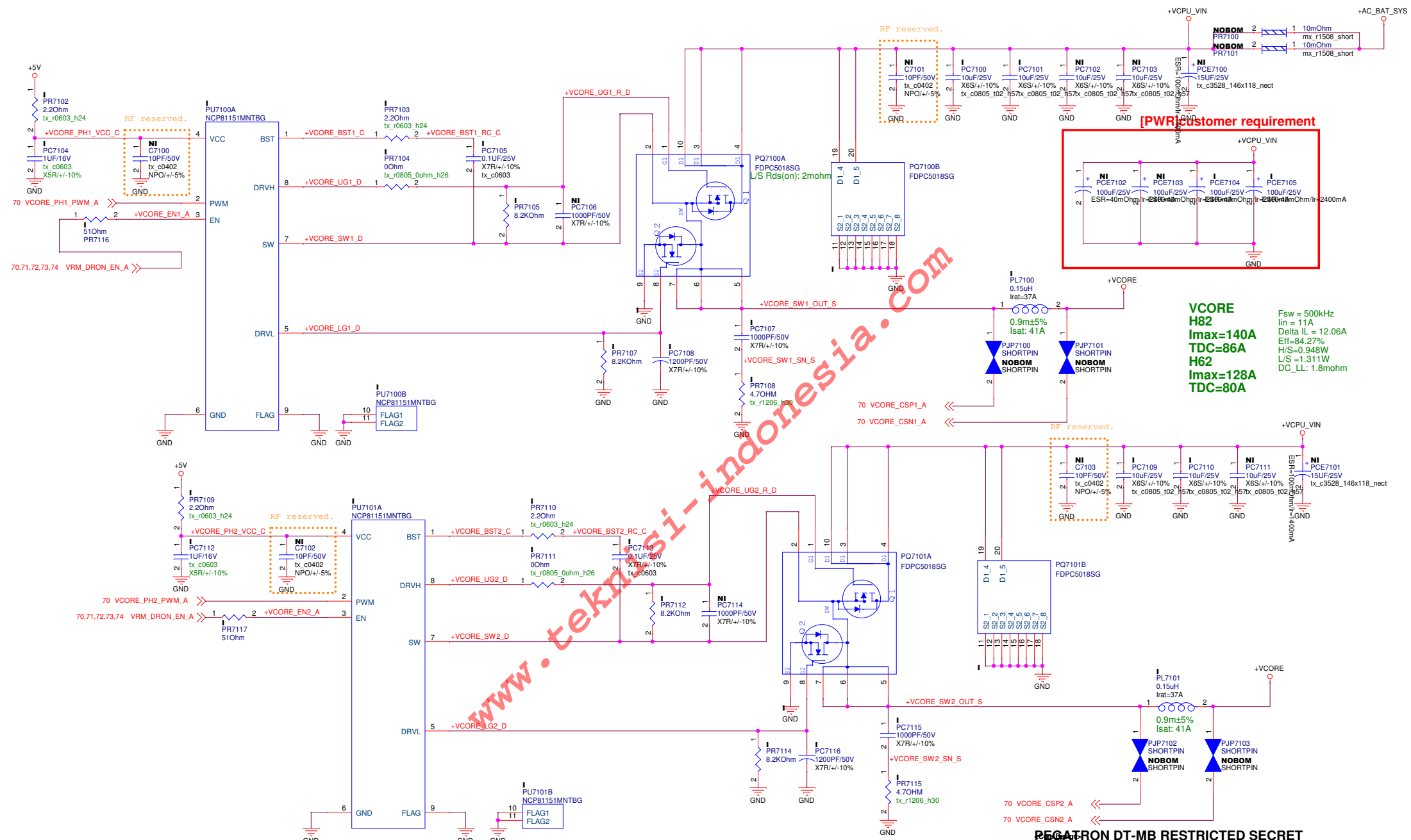
Battery Pack connector

X00a 5/22 changes to G/F type



B01 3/29 Remove Inverting Circuit



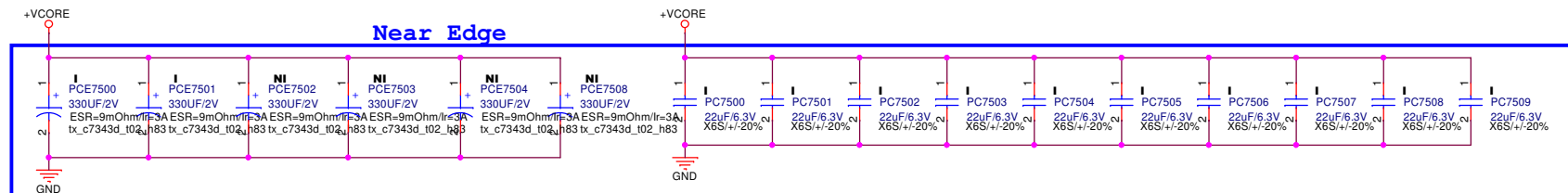


Vcore
H82
Imax=140A
TDC=86A
H62
Imax=128A
TDC=80A

Fsw = 500kHz
Iin = 11A
Delta IL = 12.06A
Eff=84.27%
H/S=0.948W
L/S = 1.311W
DC_LL= 1.8mohm

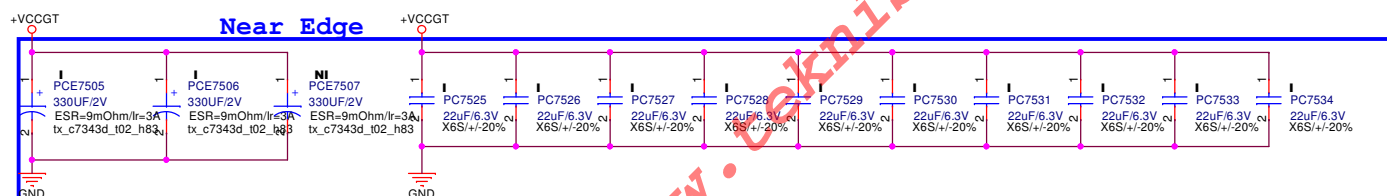
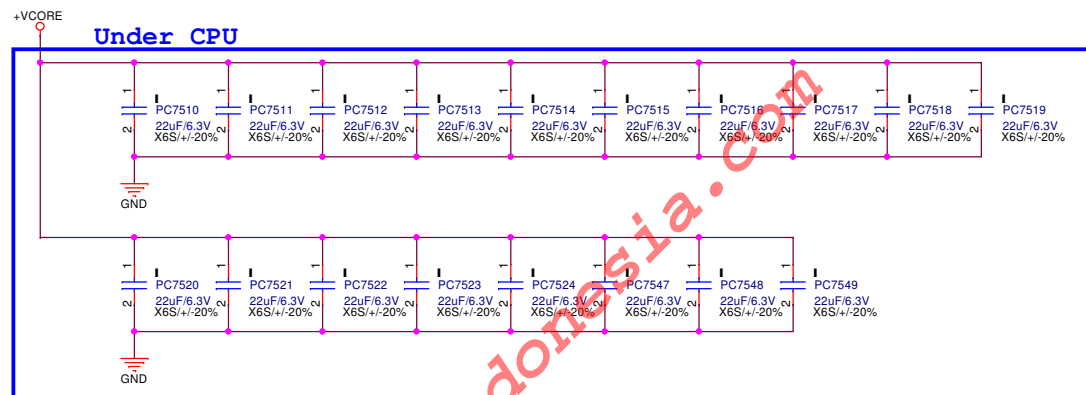
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : Vcore Driver-1	
Pegatron Corp.		Engineer: Adam Chiu	
Size	Project Name	Orion_N18E	Rev
Custom			
Date: Friday, December 14, 2018		Sheet	71 of 93



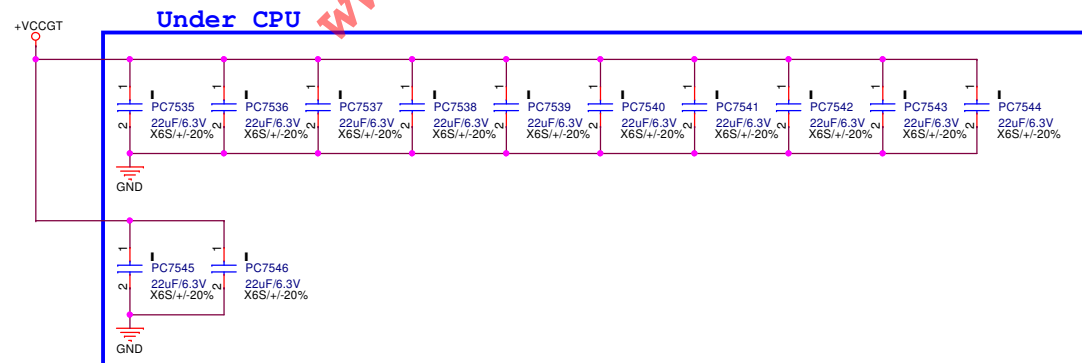
Vcore Output CAP

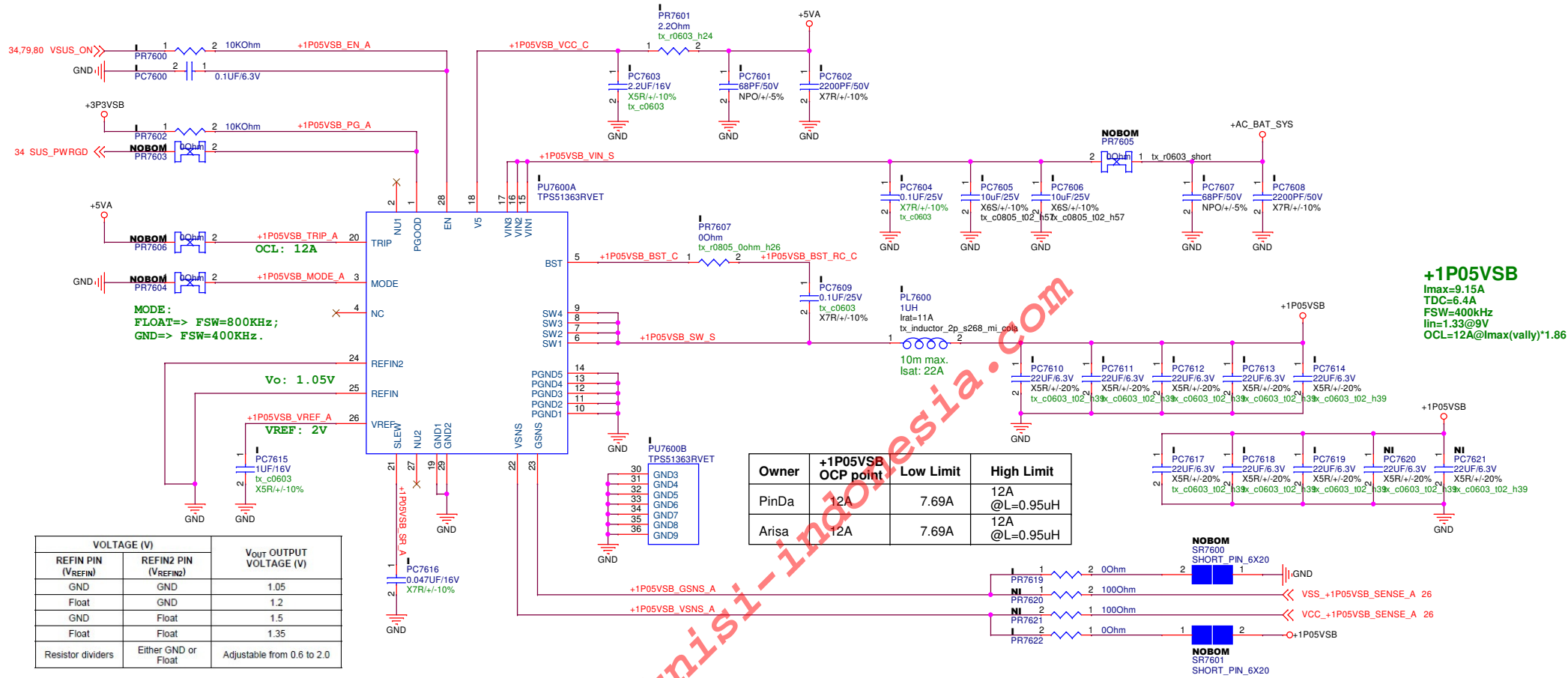
330uF/2V * 4 pcs
22uF/6.3V * 28pcs



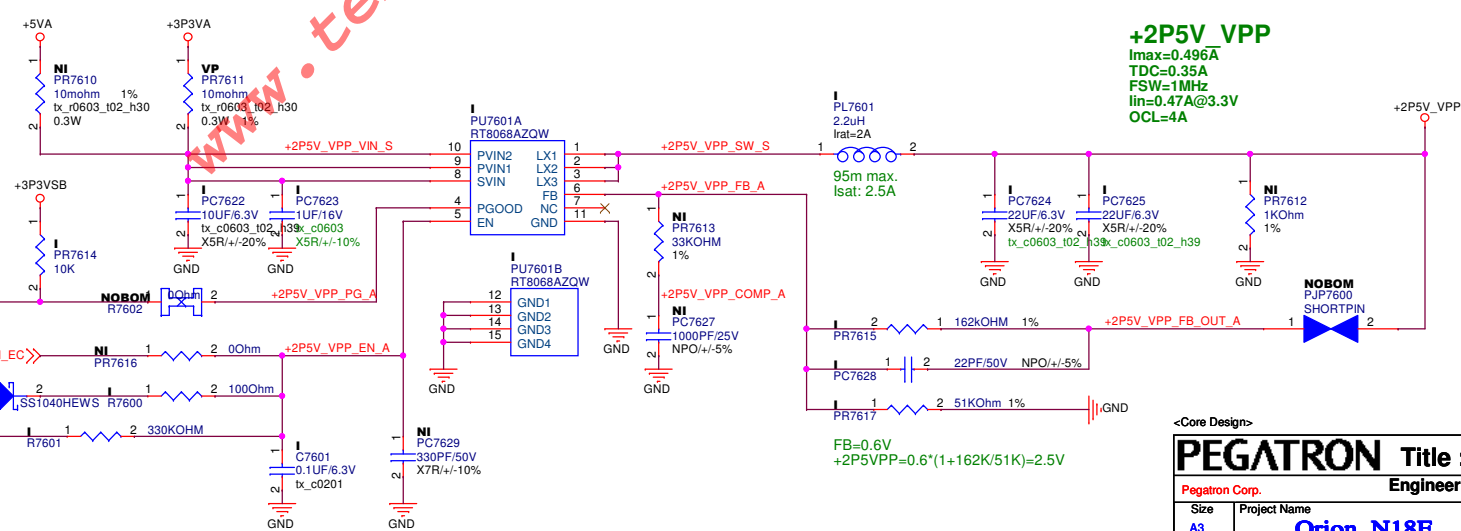
VCCGT Output CAP

330uF/2V * 3
22uF/6.3V * 22 pcs





Owner	+2P5V_VPP OCP point	Low Limit	High Limit
PinDa	4A	0.34A	4A @L=1.1uH
Arisa	4A	0.34A	4A @L=1.1uH

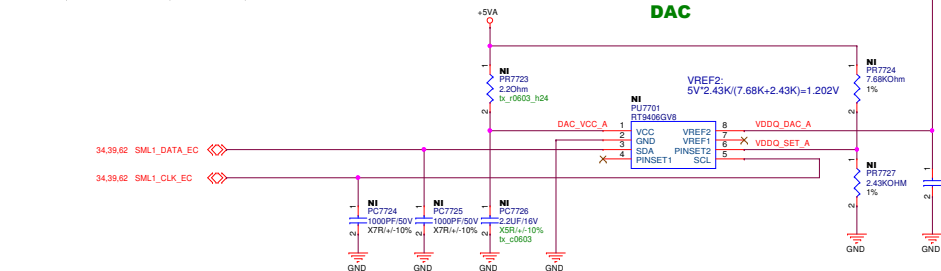


+VTT_DDR
Imax: 1.5A
TDC: 1.05A

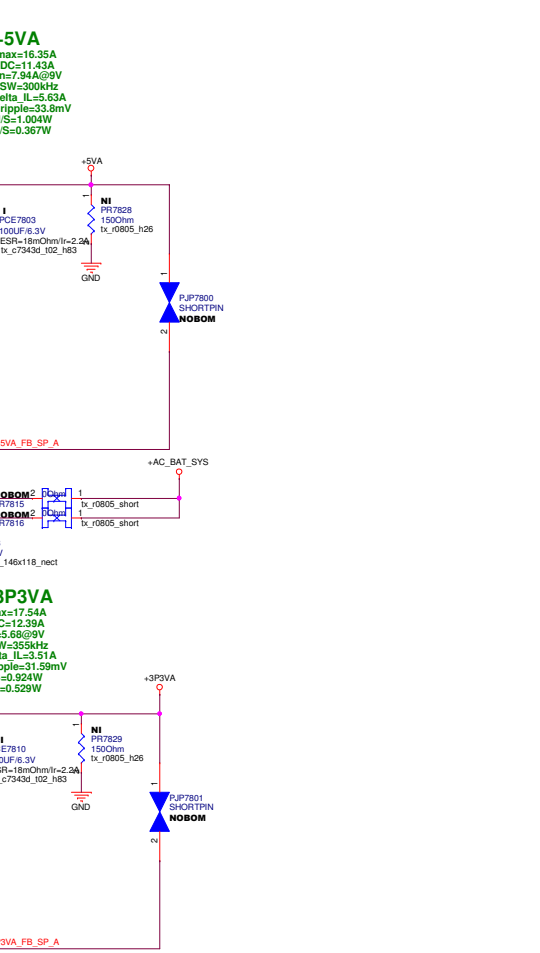
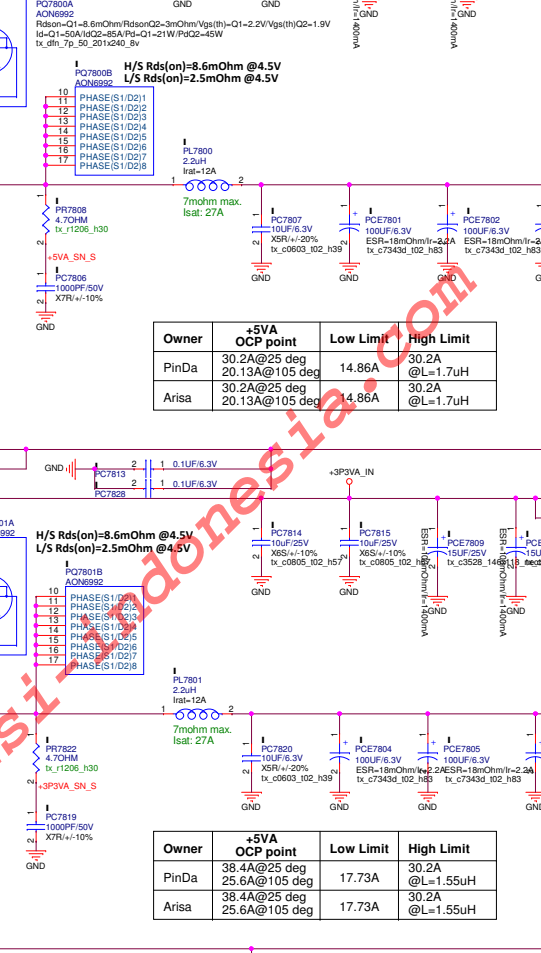
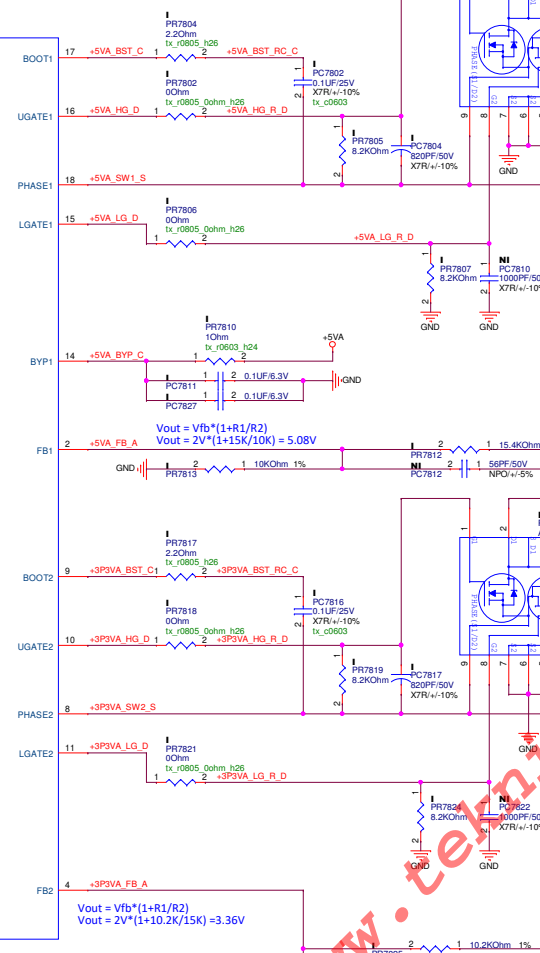
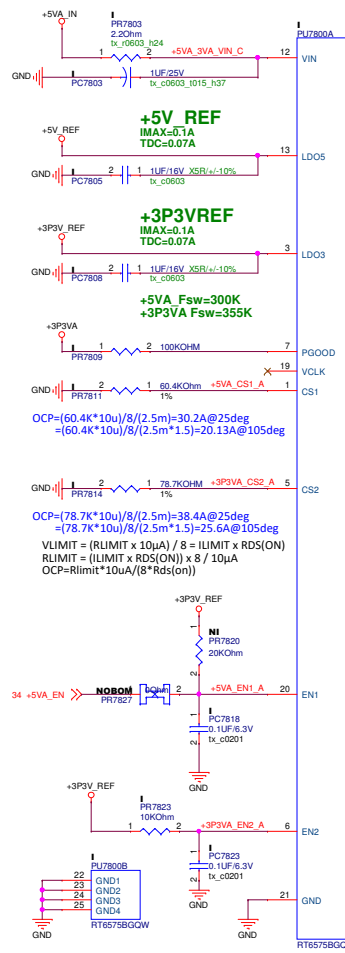
VTT LDO: 2A

OCP:
=75K*10u/8/(3m*1.3)*(7.99/2)= 28.03A@105 deg
=75K*10u/8/3m*(7.99/2)= 35.24A@25 deg

Owner	+1P2V_DUAL OCP point	Low Limit	High Limit
PinDa	35.24A@25 deg 28.03A@105 deg	16A	35.24A @L=0.32uH
Arisa	35.24A@25 deg 28.03A@105 deg	16A	35.24A @L=0.32uH

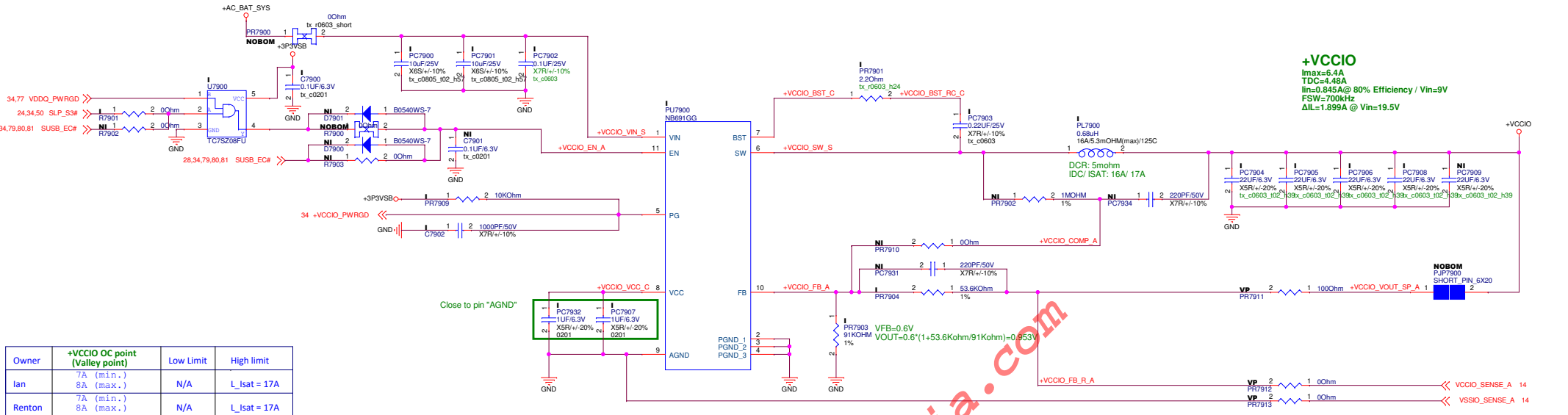


+1P2V_DUAL
Imax=15.86A
TDC=11.13A
Ilim=2.5@9V
FSW=3000Hz
delta_IL=7.99A
Vripple=35.94mV
NIS=0.427W
LS=0.653W

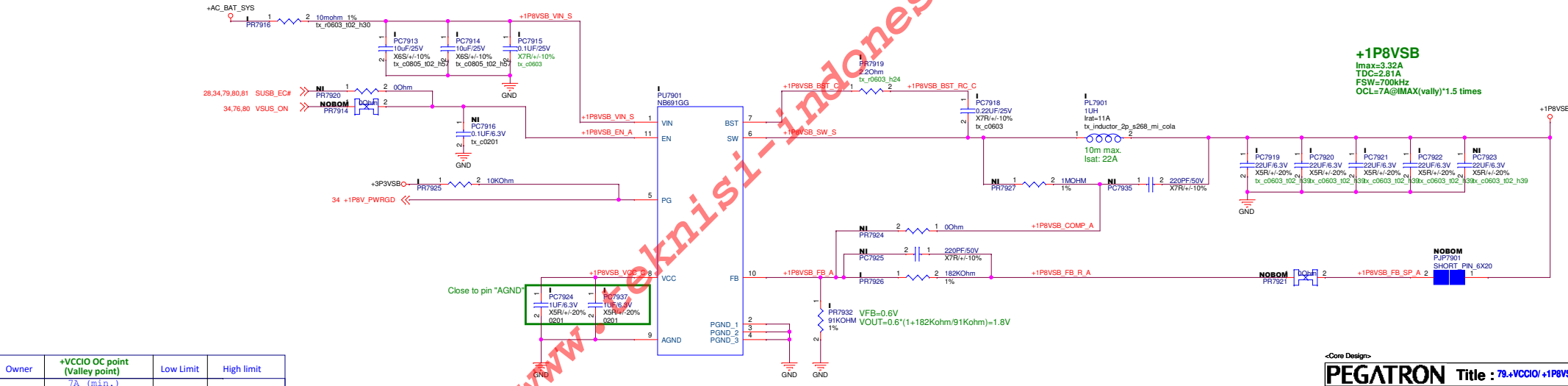


Owner	+5V OCP point	Low Limit	High Limit
PinDa	30.2A@25 deg 20.13A@105 deg	14.86A	30.2A @L=1.7uH
Arisa	30.2A@25 deg 20.13A@105 deg	14.86A	30.2A @L=1.7uH

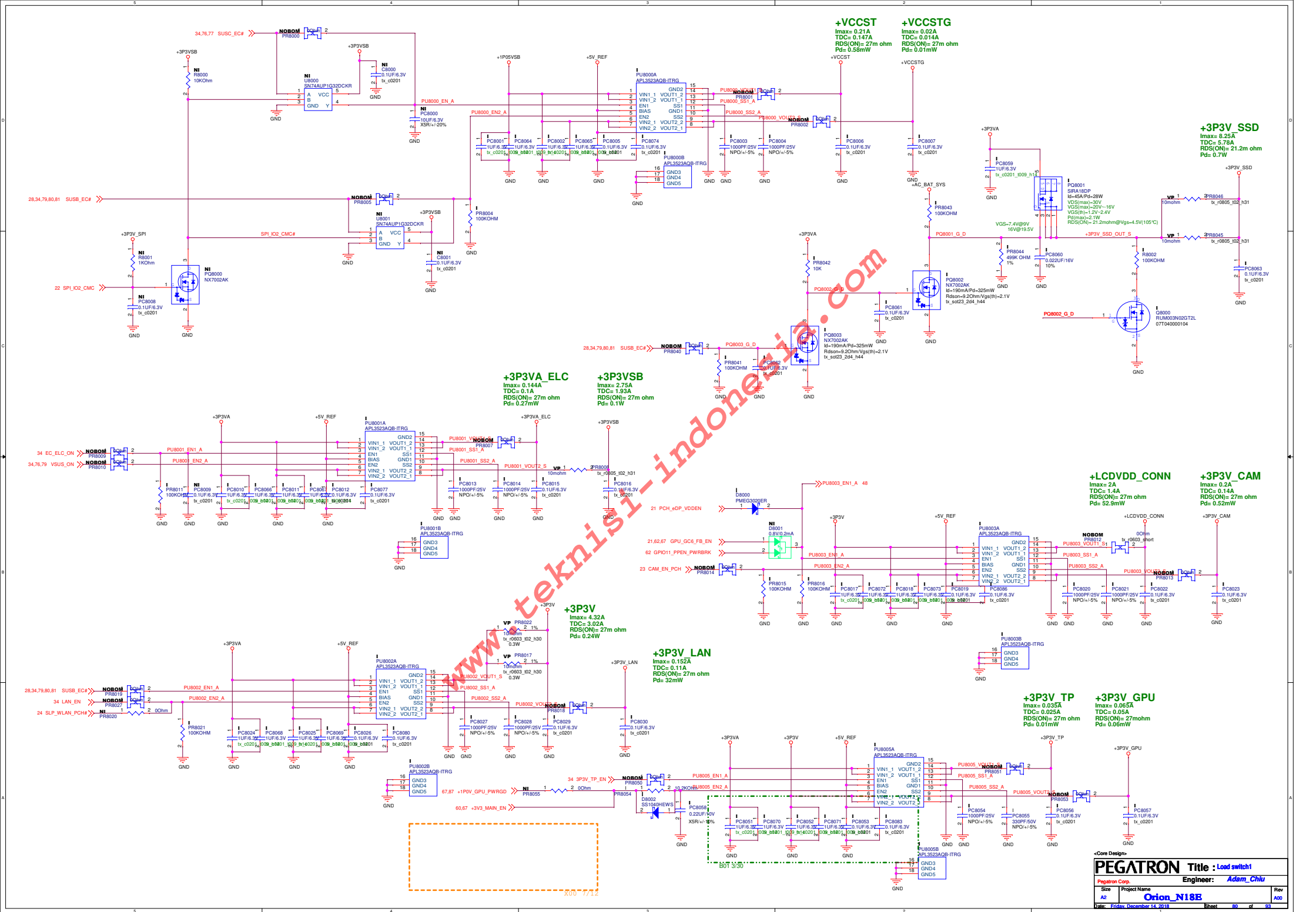
Owner	+5V OCP point	Low Limit	High Limit
PinDa	38.4A@25 deg 25.6A@105 deg	17.73A	30.2A @L=1.55uH
Arisa	38.4A@25 deg 25.6A@105 deg	17.73A	30.2A @L=1.55uH

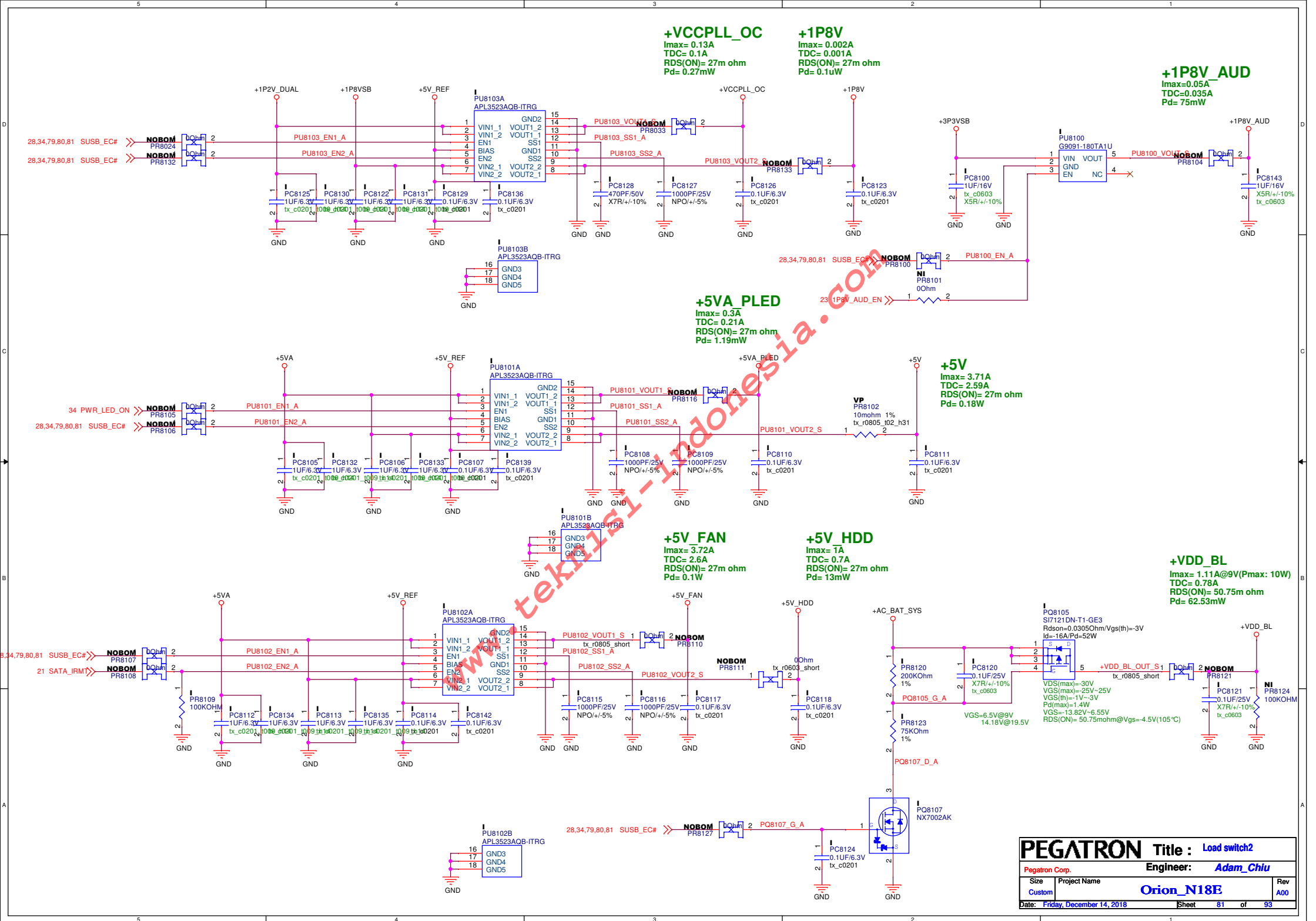


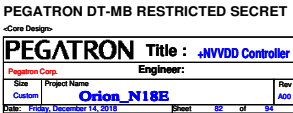
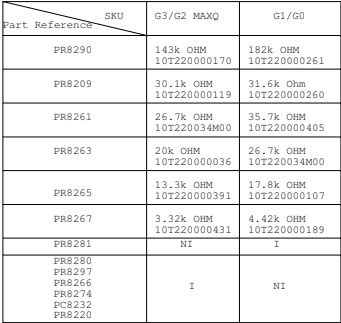
Owner	+VCCIO OC point (Valley point)	Low Limit	High limit
Ian	7A (min.) 8A (max.)	N/A	L_Isat = 17A
Renton	7A (min.) 8A (max.)	N/A	L_Isat = 17A

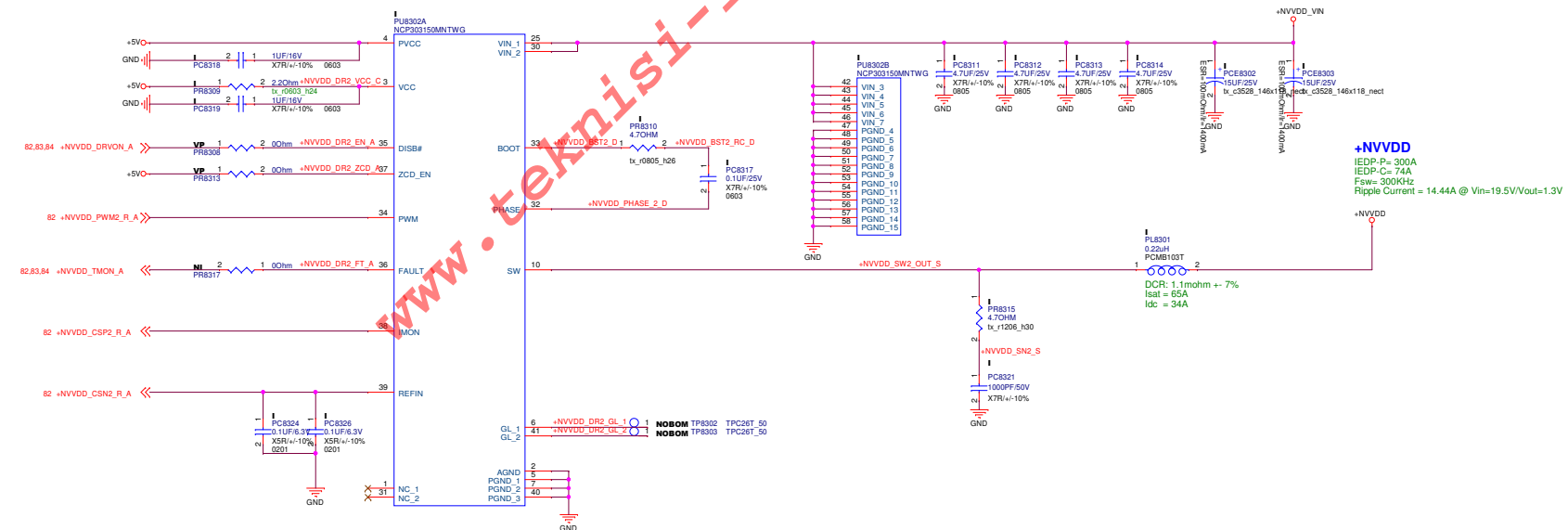
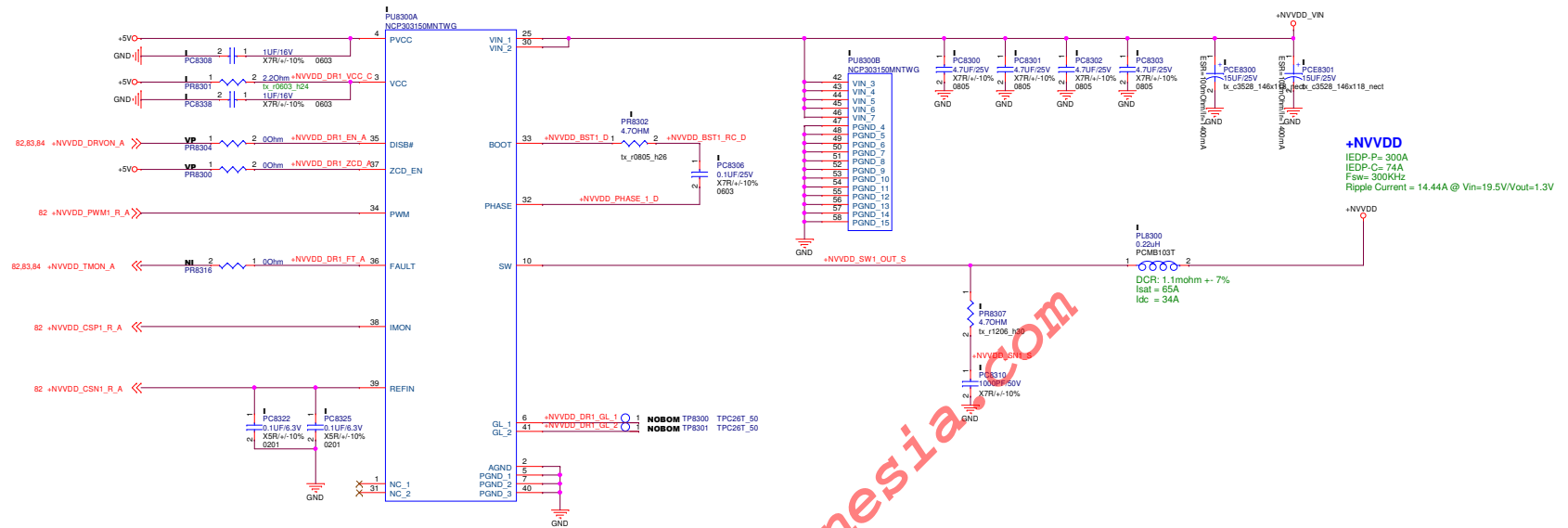


Owner	+VCCIO OC point (Valley point)	Low Limit	High limit
Ian	7A (min.) 8A (max.)	N/A	L_Isat = 22A
Renton	7A (min.) 8A (max.)	N/A	L_Isat = 22A









PEGATRON DT-MB RESTRICTED SECRET

Core Design:

PEGATRON		Title : NVVDD Driver Cap	
Pegatron Corp.		Engineer:	
Size	Project Name	Rev	Rev
A2	Orion N18E	A00	A00
Date: Friday, December 14, 2018		Sheet	63 of 94

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+NVVDDS(merge to NVVDD)

IEDP-P= 53.7A
IEDP-C= 27A
Fsw= 305KHz
Delta I= 15.68A
Vripple= 35.29mV
H/S= 0.546W
L/S= 0.7W

<Core Design>

PEGATRON

Title : xxxxxx

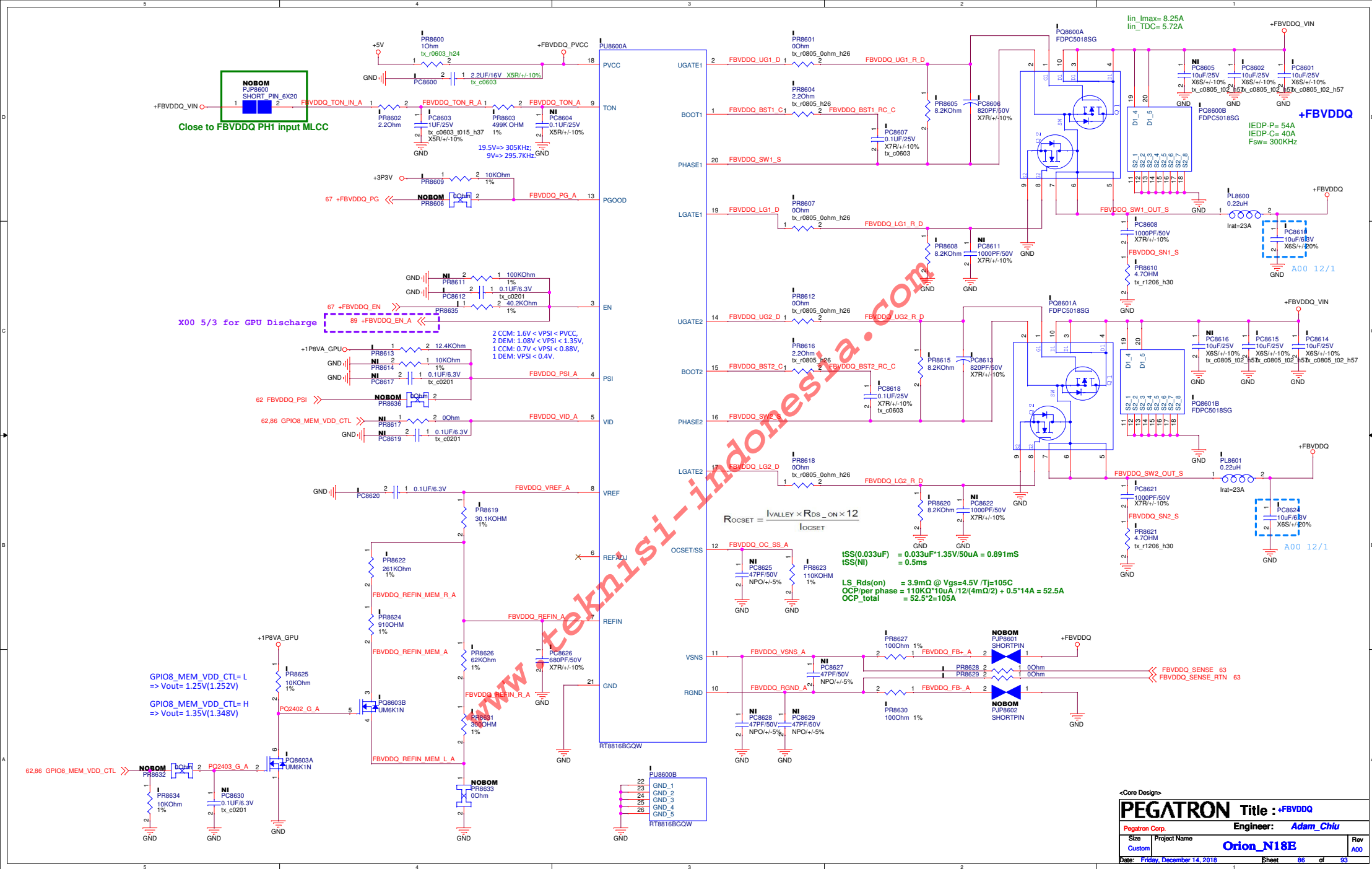
Pegatron Corp.

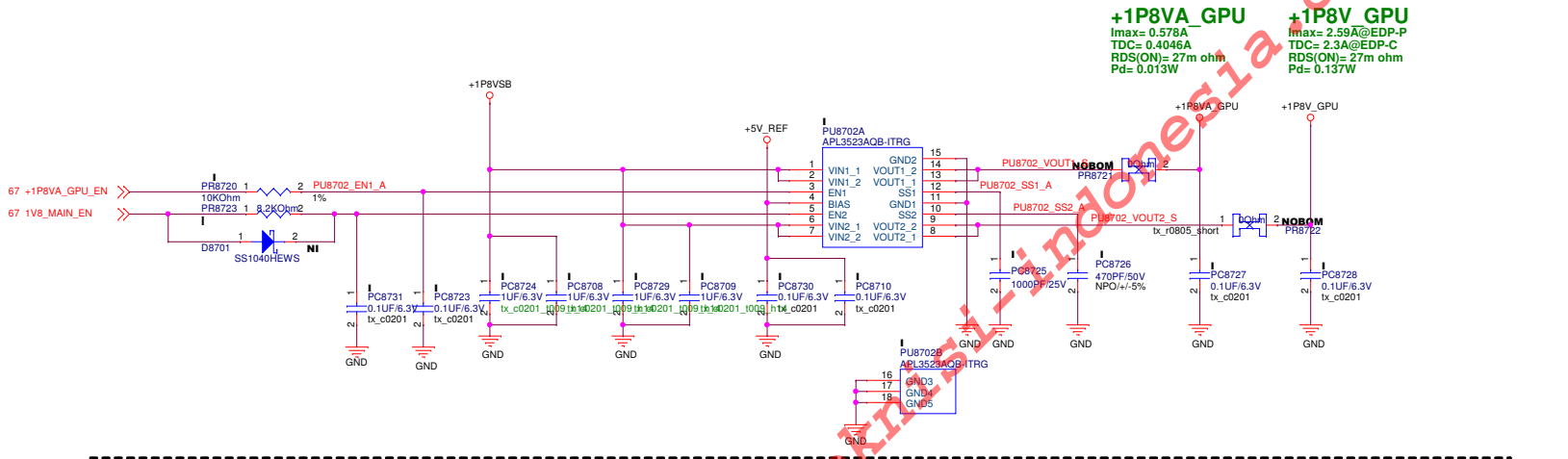
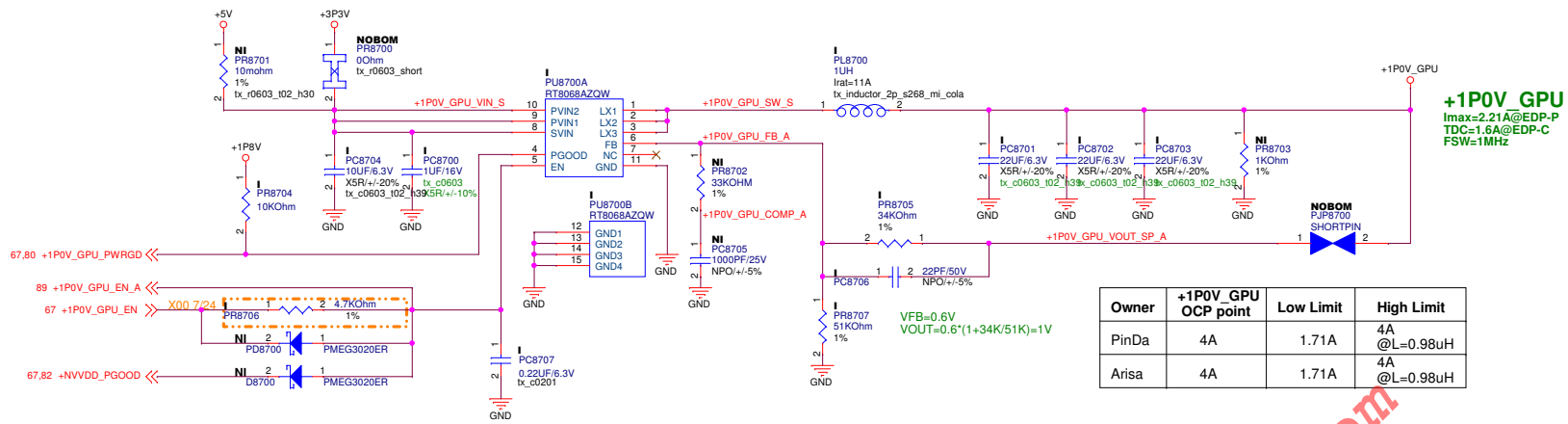
Engineer: Adam_Chlu

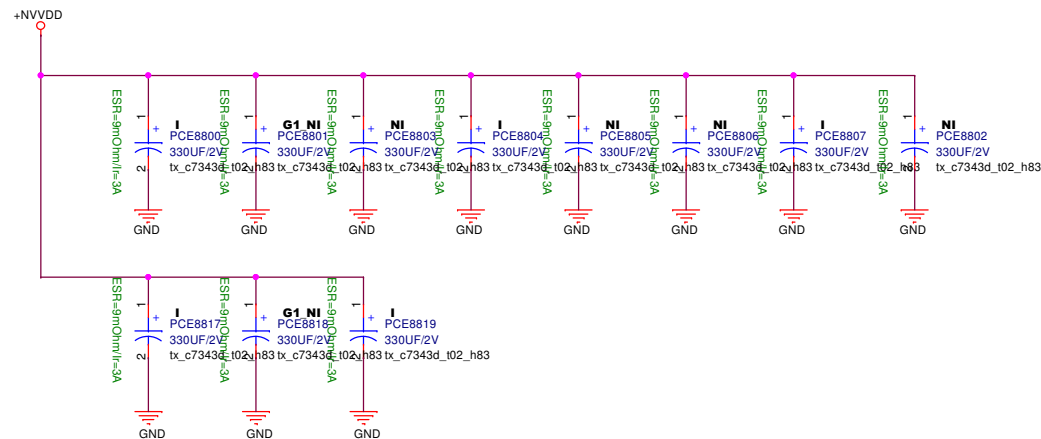
Size	Project Name	Rev
A3	Orion_N18E	A00

Date: Friday, December 14, 2018

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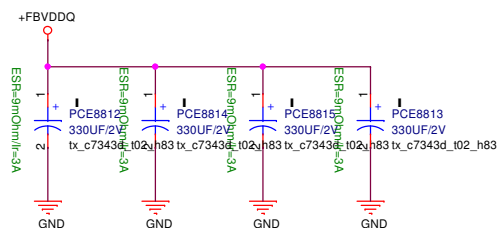






+NVVDD Output CAP

G3
330uF/2V * 7 pcs
G2
330uF/2V * 5 pcs



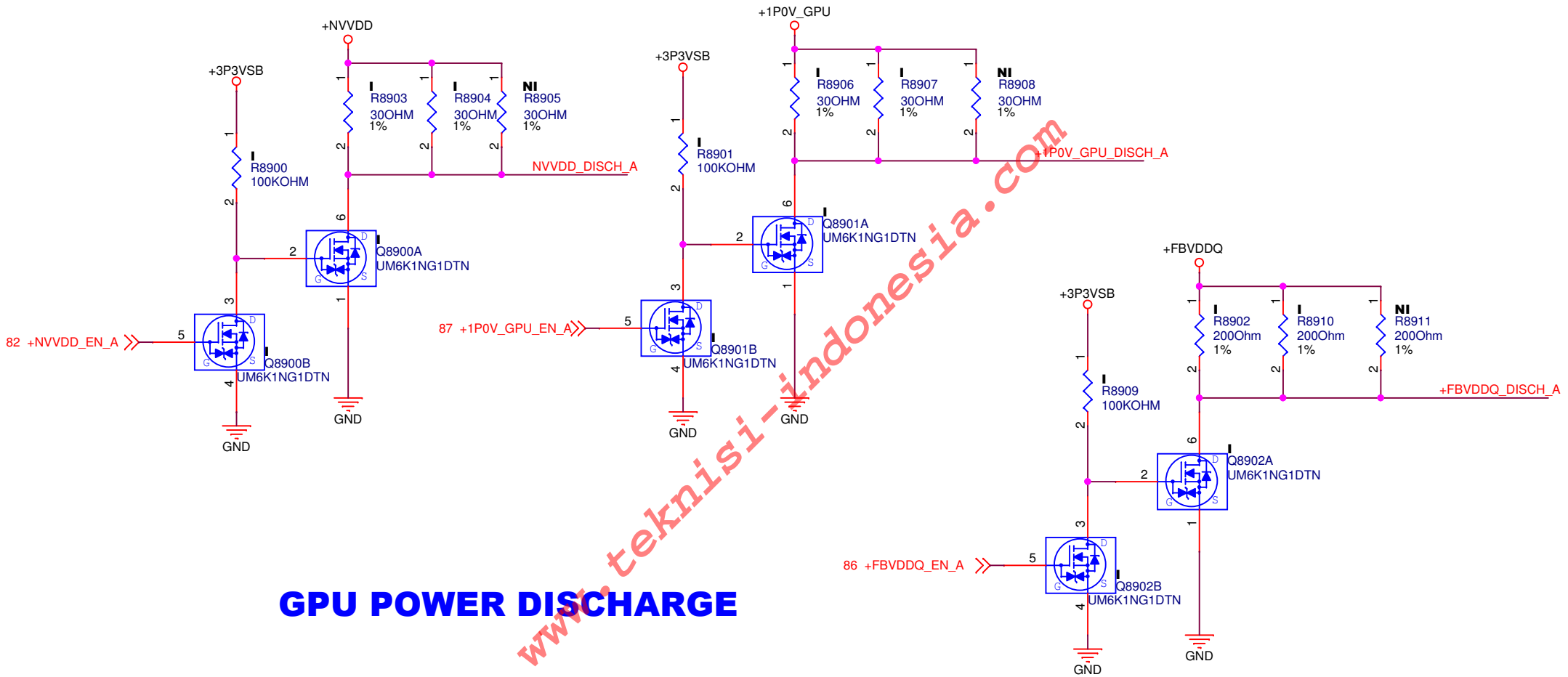
+FBVDDQ Output CAP

330uF/2V * 4 pcs

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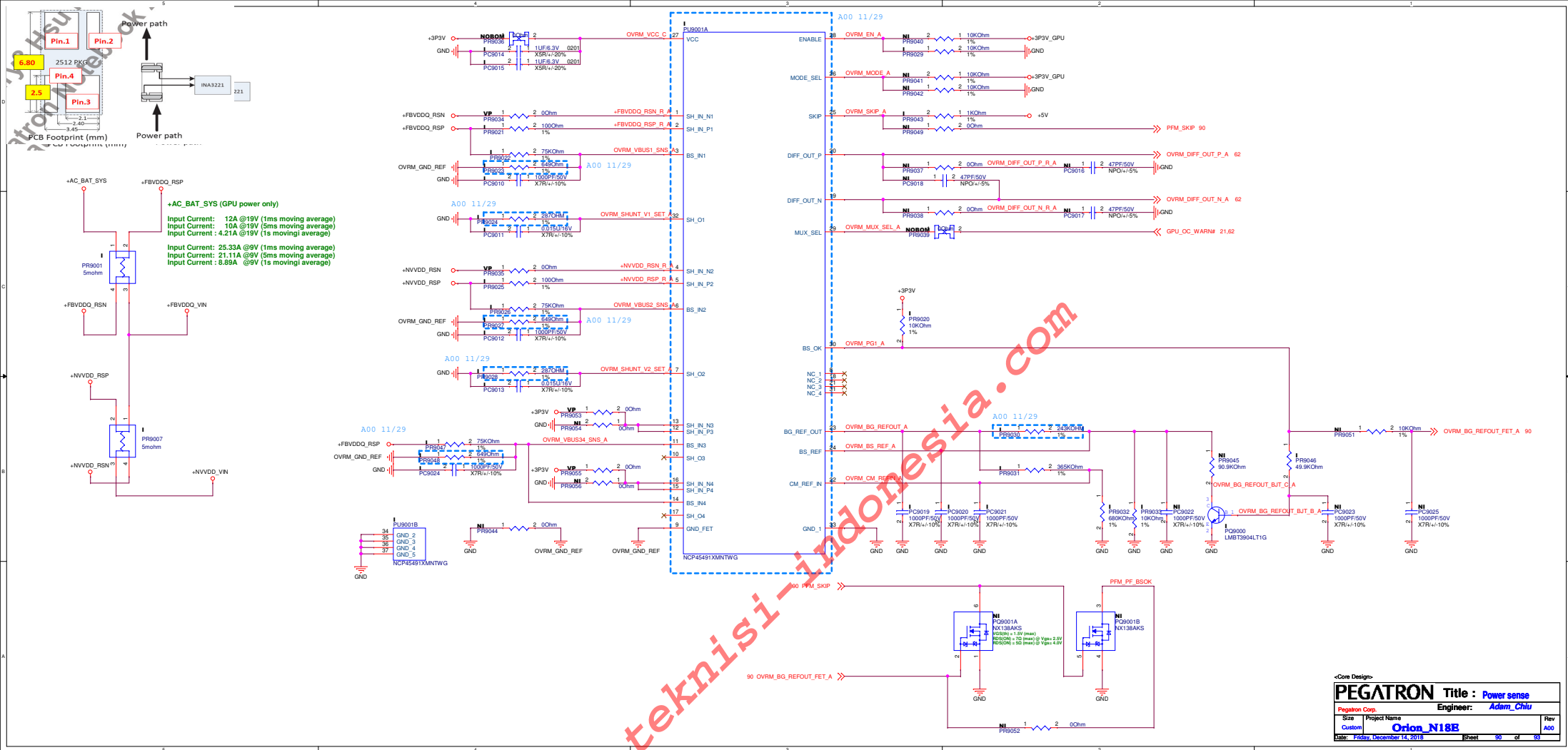
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PEGATRON		Title : GPU_POWER_CAP	
Pegatron Corp.		Engineer: Adam Chiu	
Size	Project Name	Orion_N18E	Rev
A3			A00
Date: Friday, December 14, 2018		Sheet 88 of 93	



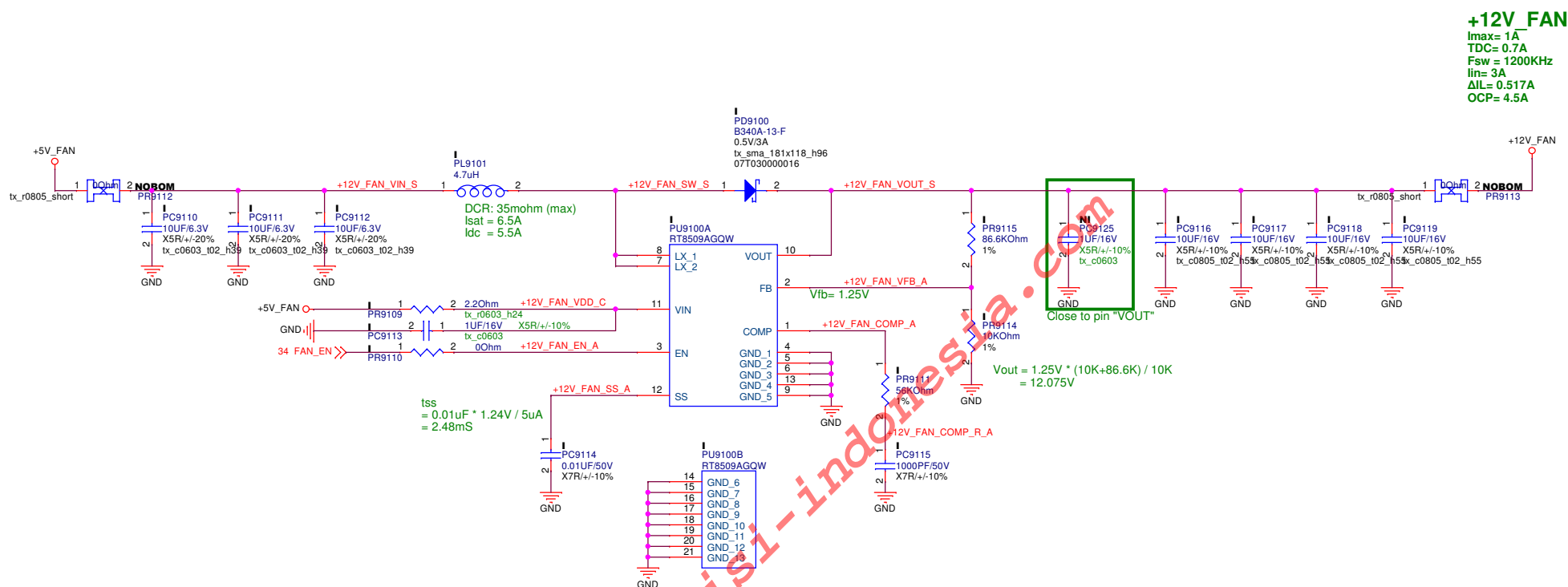
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PEGATRON		Title : GPU POWER DISCHARGE	
Pegatron Corp.		Engineer: Adam Chiu	
Size A4	Project Name Orion_N18E		Rev A00
Date: Friday, December 14, 2018		Sheet	89 of 94



<Core Design>

PEGATRON		Title : Power sense	
Pegatron Corp.		Engineer: Adam Chiu	
Size	Project Name	Rev	
Custom	Orion_N18E	A00	
Date: Friday, December 14, 2018	Sheet	90	of 93



<Core Design>

PEGATRON		Title : +12V_FAN	
Pegatron Corp.		Engineer: Adam_Chlu	
Size A3	Project Name	Orion_N18E	
Date: Friday, December 14, 2018	Sheet	91	of 93

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<Core Design>

PEGATRON

Title : xxxxxx

Pegatron Corp.

Engineer: Adam_ChIU

Size	Project Name	Rev
A4	Orion_N18E	A00

Date: Friday, December 14, 2018

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